International Journal of Computing and Digital Systems
ISSN (2210-142X)
Int. J. Com. Dig. Sys.14, No.1 (Jul-23)

http://dx.doi.org/10.12785/ijcds/140110

Design of Low Power Arithmetic Logic Unit Using SHE Assisted STT/MTJ

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Received 9 Jun. 2022, Revised 6 May. 2023, Accepted 17 Jun. 2023, Published 1 Jul. 2023

Abstract: As CMOS technology shrinks to the deep submicron range, increased power dissipation becomes a big issue. Due to its non-volatility, fast speed, great durability, CMOS compatibility, and low power consumption, the Spin transfer torque (STT) switching mechanism based on Magnetic tunnel Junction (MTJ) is widely regarded as one of the most promising spintronic devices for the post-CMOS era. The research presented here proposes a novel Arithmetic Logic Unit (ALU) that makes use of Spin Hall Effect (SHE) to aid with STT/ MTJ. In this study, we use SHE-assisted STT logic to create a Hybrid Full Adder and three other logics (AND, OR, and XOR). The proposed logics are then used to create an adder circuit, which is used to create an Arithmetic Logic Unit (ALU). A comparison of each of the proposed designs to the $DPTL - C^2MOS - ALU$ and P-MALU has been performed. The simulation findings show that the proposed designs outperform competing ALU designs, with a 28% reduction in power consumption and a corresponding reduction in latency. For circuit simulation in 45nm technology, the Cadence Virtuoso tool is employed.

Keywords: Arithmetic Logic Unit , Spin Transfer Torque , Magnetic Tunnel Junction, Spin Hall Effect

1. Introduction

High-performance portable electronic gadgets are prevalent in today's information and technology era. The speed and power consumption of these devices have a significant impact on their performance. Such devices require highly proficient circuit designs that are also efficient at lower node technology. There is a lot of research happening to develop these tools. These devices must also scale according to Moore's law. Power dissipation has risen as transistor sizes have shrunk. This means that current studies focus on developing low-power circuits with great performance. The Spintronic Device with MTJ , which uses STT switching method , has recently garnered a lot of attention due to its low voltage drop, nonvolatility, simplicity of integrating with CMOS technology, quick reading ability, and indefinite endurance [1]. Because of advances in technology like 3 dimensional back-end processes, MTJ devices could be grown on upper end of silicon semiconductor. This makes the size of the whole circuit smaller[2], [3], [4].

By adjusting the barrier thickness of MTJs, their resistance may be simply controlled to kilo-ohms, making them entirely compatible with current CMOS technology. By using MTJ, the circuit becomes non-volatile in general. Initially, MTJs were used for non-volatile memories, but subsequent research has revealed that they can be used in a variety of circuit designs. Additional spintronic devices include SPIN-transistors, domain wall (DW) based magnetic nanowires, all spin logic devices (ASLD), spin valves, 3-D magnetic ratchets, ferroelectric tunnel junctions (FTJ), and so on [5], [6], [7], [8]. These devices are utilised to design circuits and applications.

All of these spintronic devices make use of spin movement as well as electron charge. Guo et al. [9] proposed a ground-breaking magnetic ALU with a hybrid STT-MTJ/CMOS architecture. For hybrid circuit simulation, we employed a 45 nm CMOS technology[10] and the SHE assisted STT-MTJ electrical model [11]. As a first step in developing a magnetic ALU, we adopted a logic-in-memory (LIM) structure, which may also be done by altering the Guo et al. original structure of the 1-bit MALU design [9]. Compared to their CMOS counterparts, It has been demonstrated that all combination of circuits that are mentioned in the scholarly literature require nearly no standby power dissipation and are able to stay up with current scaling trends.

With the help of innovative hybrid SHE-STT-MTJ-CMOS circuits, we suggested a LIM-based ALU. Using simulation, the proposed designs are compared to the results of the clocked CMOS ALU and the magnetic ALU, both of which are based on Double Pass Tansistor logic [12], [13] respectively. The Cadence tool with a 45nm CMOS library

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and a Magnetic Tunnel Junction model [11] is used for all hybrid SHE-STT-MTJ-CMOS circuit analysis. We utilized the 4 Transistor writing circuit that was derived from [14] in all of our hybrid circuits. All transistors in the simulation are set to their default sizes of Channel length 45 nm and channel width 120 nm. The following is a breakdown of the paper's structure: The principles of MTJ and SHE assisted STT MTJ switching mechanisms are covered in Section II, while the design and operation of a single bit ALU is covered in Section III. The comparative investigation and the results obtained for various ALUs are discussed in depth in Section IV. The conclusion and future work is offered in section V.

2. Background

A. Magnetic Tunnel Junction(MTJ)

As can be seen in Figure 1, the Magnetic Tunnel Junction consists of two Ferro magnetic (FM) layers that are separated by a relatively thin oxide barrier. The direction of the magnet spin on one layer is fixed and the direction of the other spin may be changed [15]. If the direction of spin of the two FM layers are the same, then the MTJ will be in the parallel mode (P) with a resistance of R_P. If this is not the case, then the MTJ will be in the anti-parallel mode (AP) with a resistance of R_{AP}. According to research, the MTJ shows significantly more resistance in AP mode than in P mode. This behavior is cohesive tunnelling. The difference between R_P and R_{AP} is called tunnel magnetoresistance (TMR) as shown in equation 1.

$$TMR = \frac{R_{AP} - R_P}{R_P} \tag{1}$$

Since the read current in STT- MRAM follows the same path as the write current, and the read current is smaller than the write current. Read current is unidirectional and affected by magnetization of MTJ cell [16]. MTJ resistance and TMR values should change proportionally to give better results. As a result, many researchers have concentrated their efforts on developing novel materials and production techniques in order to reach greater TMR values [17]. Data retention period is an additional important feature of MTJs that are device-level attributes. In order to calculate the data retention time, known as Tstore, equation 2 is employed, where f stands for the thermal attempt frequency and δ stands for the magnetization stability energy height.

$$T_{store} = \frac{1}{f} e^{\delta} \tag{2}$$

There are many different ways of reconfiguring and data storing methods based on the MTJ structure. Field-inducing magnetization (FIMS) [18], Thermal aided switching [19], STT and Spin-hall supporting STT (STT-SHE) [20], [21], [22], [23], [24], [25], [26] are among the most practical approaches. The STT-SHE approach delivers superior performance and lower energy consumption than other methods.

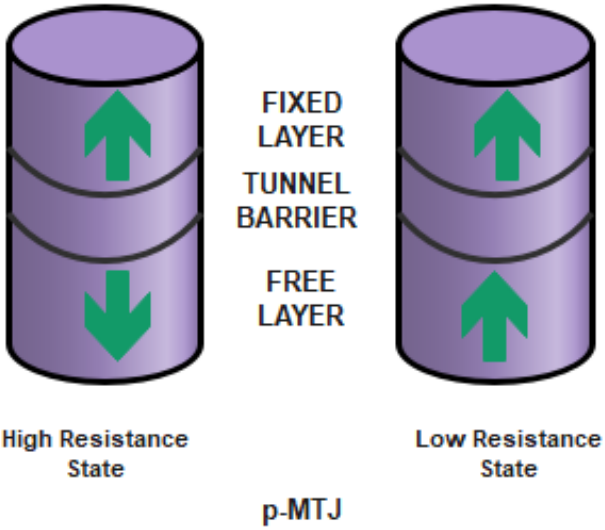

Figure 1. Prototype of a MTJ resistance

B. SHE Assisted STT/ MTJ Switching Technique

The MTJ resistance can be changed from antiparallel to parallel state or Parallel to antiparallel by adjusting the magnetic direction of the free layer. Writing/storing data in MTJ is called the MTJ switching process. FIMS demands a high switching current and consumes more energy. In FIMS, Scalability of the switching circuit was also a major issue below 90 nm because it required a prominent area on silicon. TAS solves the FIMS switching problem by adding a second heating circuit, despite the fact that it necessitates a huge silicon area. When FIMS and TAS approaches are used together, the flexibility of the MTJ writing circuit is limited. For SHE based circuits, low write current is required. As a result, ALU circuits have been designed using the SHE-aided STT (SHE+STT) MTJ mechanism. In Classical SHE devices, a heafty spin Hall metal (SHM) and an MTJ is synthesized on above the metal wire. As seen in equation (3), the magnetization dynamics of the MTJ's free layer can be described by a modified Landau-Lifshitz-Gilbert (LLG) equation [14] for spin-Hall-assisted STT switching.

$$\frac{\partial m}{\partial t} = -\gamma\mu_0 m\chi H_{eff} + \alpha m\chi \frac{\partial m}{\partial t} - \epsilon P J_{STT} m\chi(m\chi m_r) - \epsilon n J_{SHE} m\chi(m\chi \sigma_{SHE}) \tag{3}$$

Where m represents unit vector in the direction of magnetic orientation of free layer and m_r unit vectors along reference layer's magnetization orientations. J_{STT} stands for write current density of STT and J_{SHE} stands for write current density of SHE. H_{eff} is the most effective coefficient as it contains external field as anisotropic, magnetostatic. [14] has further information on the other coefficients. According to numerical modeling based on equation 3, two conditions must hold for quick switching of STT with the help of SHE: i) J_{SHE} needs to be as high as to be able to provide high spin-Hall torque. ii) in order for STT to maintain

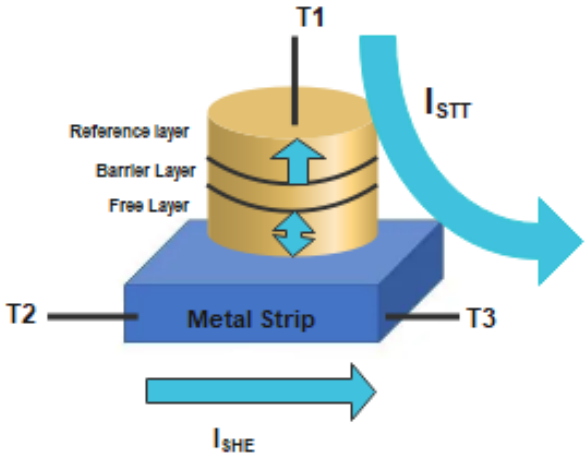

Figure 2. MTJ device assisted with SHE

deterministic switching, J_{SHE} must be withdrawn at the proper moment. In [17], a model of the upcoming spin-Hall aided MTJ that can be run in spice has been developed. The LLG equation [14] is used to characterise tunnelling resistance and switching of magnetization, in addition to the Brinkman model and the Slonczewski model. It mediates between MTJ signals and CMOS circuitry and is built in the Verilog-A computer language.

C. Hybrid MTJ/ CMOS Structure

The Classical Von-Neumann design separates logic and memory blocks, but cables and connections allow for connectivity between them. This method degrades the chip's overall performance. As the wire length grows, a large delay is introduced between these two blocks. In addition, with a MOSFET reducing its channel length, it has a dissipation of power supply. This enhances the complete power dissipation of the circuit. In addition, with the level of integration, standby power is said to grow. Logic in Memory is an innovative inclination that may be able to solve the problem of rising leakage currents caused by scalability and excessive connection delays in conventional design. In this hybrid LIM structure all devices are kept next to each other rather than keeping all devices on above each-other. Due to this overall area occupied is reduced, resulting in tight integration. As a result, as compared to the Von-Neumann design, there is a considerable reduction in latency and power usage[27].

The LIM structure is depicted in Figure 3 as a generic block diagram. It is divided into three sections. 1) Current Comparator/Sense Amplifier Circuit: The Sense amplifier offers output in its exact and opposite form once the pull-down network (PDN) has completed its function on the inputs. 2) Pull-down network: This is a network that combines MOS logic with MTJ. MOS logic and MTJs are used to create logical operations. 3) The writing block : is used to store the data into the MTJ. A current comparator

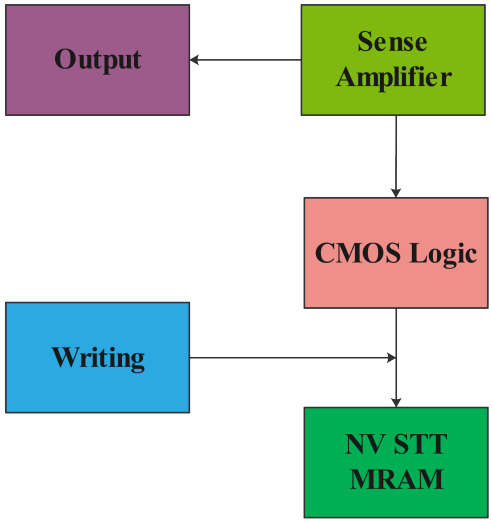

Figure 3. Hybrid MTJ structure

pre-charge sense amplifier [28] is utilized in ALU systems.

3. Design of ALU

The design and operation of Arithmetic Logic Unit circuits constructed utilizing the hybrid SHE-MTJ/CMOS LIM architecture are described in this section. To make sure that these circuits work, simulated output waveform of the corresponding circuits are also presented.

The arithmetic logic unit (ALU) is the brains of central processing unit (CPU). This component conducts both mathematical and logical computations. Block diagram of 1-bit ALU has shown in Figure 4 [13]. For arithmetic unit, Full adder circuit is designed. Full adder has two output- Sum and carry , their circuit diagram have shown in Figure 5 and 6 respectively. Full adder circuit have three inputs- C(stored in MTJ), B and A. For logical operations- XOR gate, NAND gate, NOR gate, XNOR gate, AND gate, and OR gate have designed as shown in Figure 7,8. For the operation of ALU, multiple combination of opcodes have been used as shown in Table I . In table I, opcodes are utilized as select lines for multiplexers. With different values of opcodes, multiple operations of ALU is carried out.

When the opcode "'b1" is set "0", operation of arithmetic unit of ALU takes place. Hybrid Full adder has three inputs- C, B and A and two outputs- Carry and Sum. Input C is written in non-volatile MTJs (MTJ1, MTJ2), giving the ALU non-volatility. The sensing amplifier, CMOS logic, and MTJ pairs with SHE assessment are the three key elements of these circuits. The sense amplifier is a current comparator [28] that uses the difference in current flow on the circuit's two sides (left and right) to create true and

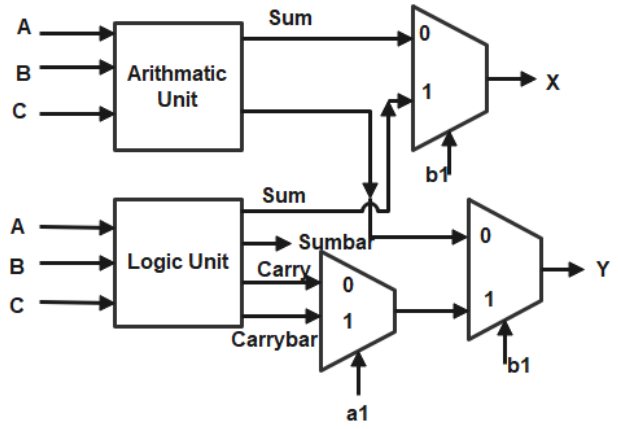

Figure 4. ALU Element

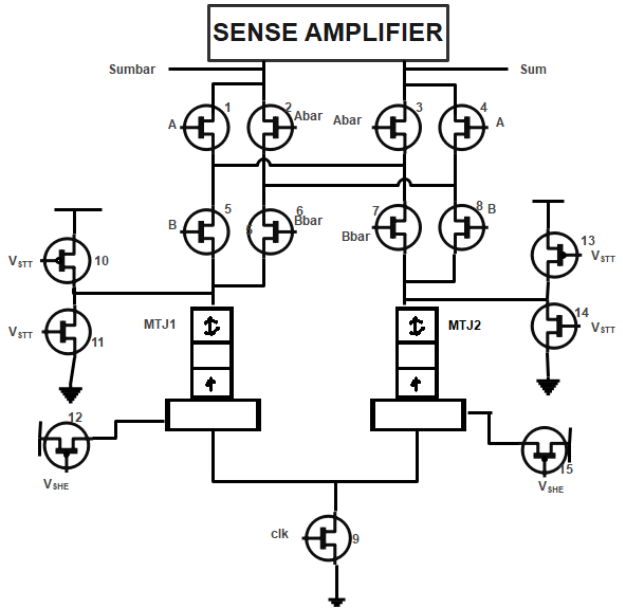

Figure 5. Proposed Hybrid Full Adder Sum Design using SHE assisted STT

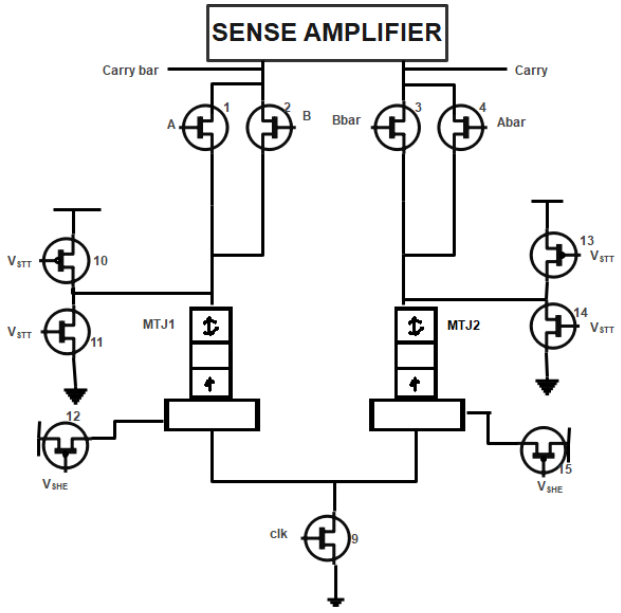

Figure 6. Proposed Hybrid Full Adder Carry Design using SHE assisted STT

complementary outputs of Sum and Carry. The NMOS in the PDN portion operates as a switch. Both MTJs will always be in complementary mode, means if MTJ1 is in parallel mode, then MTJ2 will be in antiparallel mode or vice versa, which provides a low/high resistive channel for current flow and is crucial in determining the circuit's output. The NMOS resistance is always equivalent to the MTJ resistance. The NMOS's OFF resistance (R_{OFF}) is greater than the MTJ's antiparallel state resistance (R_{AP} MTJ); $R_{OFF} > R_{AP}$ MTJ.

Table II provides the output of the full adder for the different combinations of inputs. The pre-charge phase and the assessment phase are the two phases of the adder circuit (Figure 5). When the clk signal is low, it indicates a pre-charge period, and inputs are applied to MOS logic and MTJ pairs. If the clk signal is high, that means evaluation phase. During the evaluation phase, the sensing amplifier measures the difference in flow of current between both sides of the sum / carry circuit. This current difference is determined by variations in resistance on both sides of the circuit, resulting in actual and complementary outputs. In Figure 5, There are two paths, one from the Sum to the ground and other from Sumbar to ground. The right-side path contains two ON transistors whose combined resistance is $2R_{ON}$. In the same way, the left side path has two ON transistors with a total resistance of $2R_{ON}$. The resistance of the MTJ pairs now determines the output value. When C is at logic 1, then MTJ1 is termed the Anti Parallel mode and MTJ2 is termed the Parallel mode. Under these, the left side's overall resistance is $2R_{ON} + R_{AP}$, and the right arm's total resistance is $2R_{ON} + R_P$. As a result, the current in the left side path encounters less resistance on its way to the ground than the current in the right-side path. This results in a current imbalance between the two sides of the circuit, that is sensed by the sense amplifier and translated into logic 0 and logic 1 at the sum outputs. Similarly, the carry circuit (Figure 6) generates output logic 0/logic 1. The arithmetic module's capabilities are demonstrated in Figure 9.

The entire adder circuit performs operations sum and carry based on the input operands A and B. C is a logic opcode that performs a specific logic operation. We get the sum and carry output of the full adder as shown in equation 4,5.

$$Sum = A\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}C + ABC \quad (4)$$

TABLE I. Operation in ALU

OPCODE C	a1	b1	OUTPUT X	Y	FUNCTION
X	X	0	Sum	Carry	Arithmatic
0	0	1	XOR	AND	Logical
0	1	1	XOR	NAND	
1	0	1	XNOR	OR	
1	1	1	XNOR	NOR	

TABLE II. Operation of Full adder

INPUT A	B	C	OUTPUT SUM	CARRY
1	1	1	1	1
1	1	0	0	1
1	0	1	0	1
1	0	0	1	0
0	1	1	0	1
0	1	0	1	0
0	0	1	1	0
0	0	0	0	0

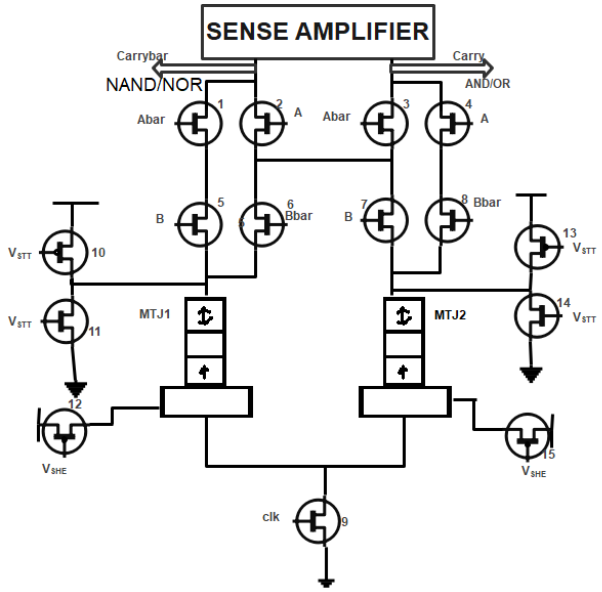

Figure 7. Proposed AND/OR logical circuit using SHE assisted STT

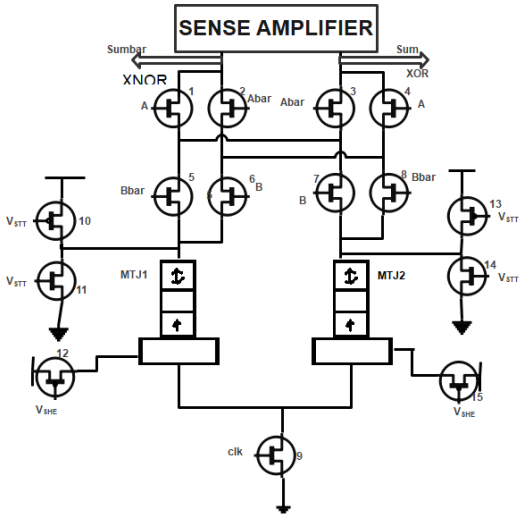

Figure 8. Proposed Hybrid XOR/XNOR logical unit using SHE assisted STT

$$Carry = AB + BC + CA \tag{5}$$

When opcode b1 is set 1 then ALU performs logical function. For different logical function – AND/OR/ NAND/NOR/ XOR/XNOR different combinations of opcode C and a1 are used (as shown in table 1). Figures 7,8 display the logical circuits of the AND/OR gate and XOR/XNOR gate. Figures 10, 11 depict the output of the logic unit.

4. Results and Discussion

Simulations of ALU circuit using SHE and MTJ models [10], [11]are shown in this section. The outcomes of proposed arithmetic and logical unit simulations are studied separately in terms of power, number of MOSFET/MTJ pairs, and latency. For the purposes of simulation, all of the suggested circuits operate at 100 MHz. The $DPTL$ –

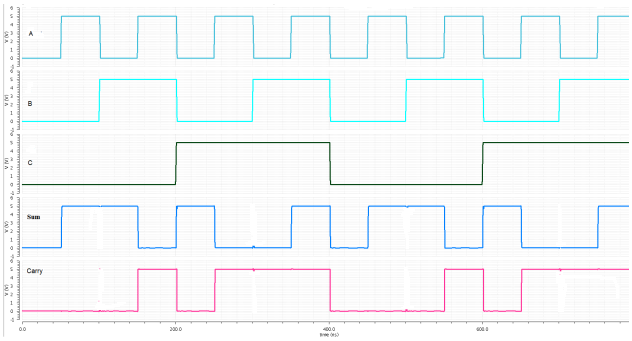

Figure 9. Output of full adder carry design when opcode b1 is set 0

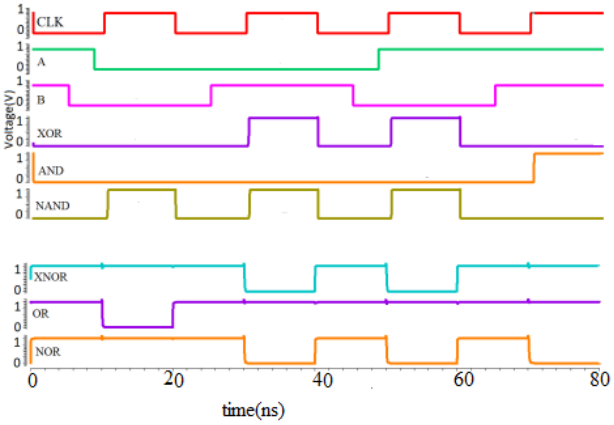

Figure 12. Simulation result of logic gates when opcode b1 is set 1

Figure 10. Simulation result of NAND logic

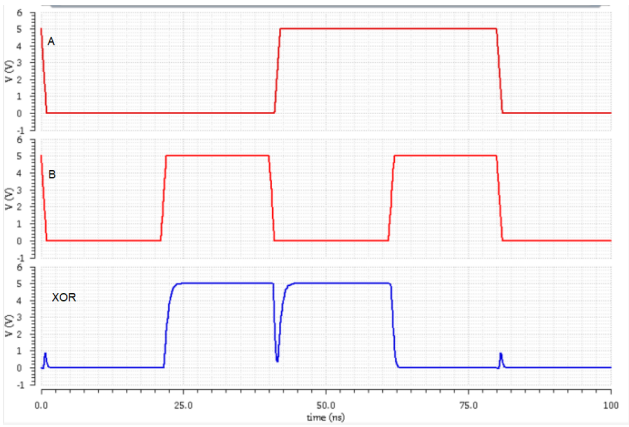

Figure 11. Simulation result of XOR gate

$C^2MOS-ALU$ [12] unit was designed using a CMOS 1-bit full adder from the STMicroelectronics design kit's standard cell library [10].

SHE-assisted STT-MTJ model version "PM Beta 5" has been chosen, which was recently constructed with Verilog-A [11]. The parameters for the SHE-assisted MTJ model[11], [14] that we employed in our simulation are listed in table III. The default settings for the other parameters are the same as in [12]. Different characteristics, such as material qualities, device dimensions, TMR etc., determine the MTJ R_P and R_{AP} resistance. This effect is taken into account in the design stage by including variations in parameters such as thickness (t_{ox}) of oxide layer, Tunnel Magneto Resistance. The resistance levels of the MTJ would be affected by changes produced by these parameter modifications. As a result, this would have an impact on the hybrid circuits' overall performance. Table IV compares the the $DPTL-C^2MOS-ALU$ [12], P-MALU [13] and the proposed ALU in terms of how much power they use, how many devices they have, and how long it takes for them to do their work.The proposed ALU adder uses 39 % less dynamic power than the $DPTL-C^2MOS-ALU$ adder and 12.5% less dynamic power than the P-MALU adder design. The ALU adder's overall power consumption is 28% lower than that of the $DPTL-C^2MOS-ALU$ adder and 16% lower than that of the P-MALU full adder. A bar chart for the power dissipation can be seen in Figure 13. For Power consumption of ALU circuit: Inputs are applied to the CMOS logic, while input C is stored in the MTJ pair. The circuit is non-volatile. It is possible to entirely disable the ALU circuit's power supply while it is in standby mode, reducing its power consumption to almost nothing. The stored bit will be retained by a pair of MTJs. Figure 14 represents the delay comparison.

The MOS transistors receive inputs A and B. The ALU generates the outputs Sum and Carry, based on ABC input combinations. At this time, the ALU circuit doesn't use

TABLE III. Simulation MTJ Parameters[11]

PARAMETER	DESCRIPTION	VALUE
Area		32nmX32nm
Jco	Critical Current Density	5.7X105 A/Cm2
V	Volume of Free Layer	Surface X 1.1nm
Heavy Metal Resistance		833 \ohm
Supply voltage		1V
Spin Hall Angle		0.3V
Heavy Metal Volume		50nmX40nmX3nm
TMR(0)	Tunnel Magneto Resistance	120%
MTJ resistance		6kohm
Tox	Thickness of Oxide Layer	1.4nm

TABLE IV. Comparision of the Proposed ALU(Hybrid Full adder with other Designs)

Parameter	$DPTL-C^2MOS-ALU$[12]	P-MALU[13]	Proposed ALU
Dynamic Power(nW)	255.2	177.9	155.6
Static Power (nW)	7.5	0	0
Total Power (nW)	262.3	187.7	160.7
Device Count	48MOS	34 MOS+4MTJ	38 MOS+4MTJ
Sum latency (ps)	56.6	48.34	26.9
Carry latency (ps)	56.7	52.3	37.8

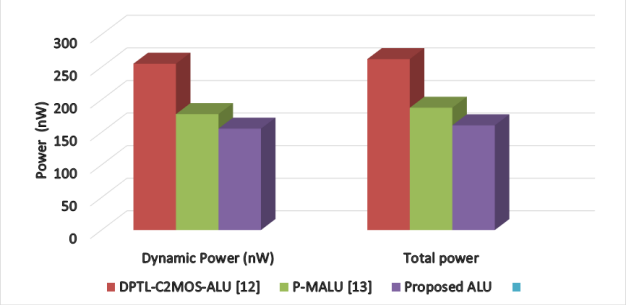

Figure 13. Comparision of Power dissipation among all ALU

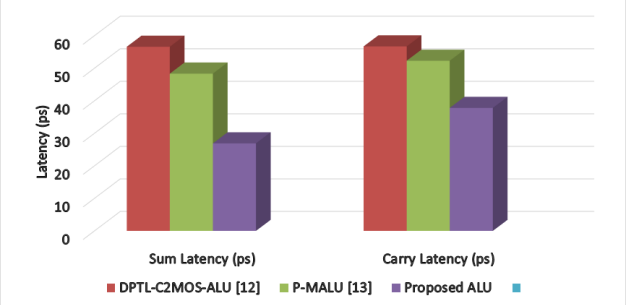

Figure 14. Comparision of Latency among all ALU

any power because MTJ isn't volatile. The MTJ pairs engage in the logic process as well as storing the logic value. The MTJs do not contribute to the additional latency in the outputs. The sense amplifier's sensing quality determines how long it takes to calculate the output of Sum circuit and Carry circuit. The device count and all other parameters of various arithmetic units are shown in Table IV. Hence, the proposed ALU outperforms the other existing designs by implementing arithmetic and logic with a far lower number of devices. As a result, the proposed ALU architecture has a significantly smaller overall die area than CMOS technology. Latency for Sum and Carry circuit is shown in Table IV. The proposed design has the smallest Sum and Carry delays than other designs. Sum and Carry circuits have four ways for any of the outputs to go to ground. During this time, neither of the MOSFETs is turned on or off. Input C is applied through MOSFETs in $DPTL-C^2MOS-ALU$ [12], resulting in a longer delay. Hence, $DPTL-C^2MOS-ALU$ [12] and P-MALU [13] have a longer delay than the proposed ALU. The output delay in a suggested ALU system is determined by the dimensions of the pull-down transistor. In the variation of channel width from 120 nm to 480 nm, reduction in latency takes place. This is owing to the bigger channel, which allows for a faster discharge of current. Meanwhile, the larger transistor will consume more area on the entire circuit.

5. Conclusions and Future Work

In academia and industry, a great deal of research is being done to create innovative designs based on the STT-MTJ/CMOS hybrid framework. In this study, a novel ALU design using SHE-assisted STT-MTJ/CMOS is proposed, and it is found to be superior in terms of power consumption, number of MOSFETs, and latency. Proposed circuits have a substantial benefit over volatile CMOS designs in this regard. According to the findings presented in this study, the proposed architecture not only consumes less

power but also takes up less space on silicon. As a result, ALU design offers a lot of potential in low-power VLSI circuits that also take into account post-CMOS scaling trends. In this work, we suggest the design of a 1-bit ALU. Future work can take advantage of the possibility of designing ALUs with four or more bits, allowing for higher-bit calculations. Other full adders, such as the ripple carry adder or etc., can be designed within the context of a full adder. Every single one of the proposed layouts utilises a 100 MHz frequency. In this way, the effects of frequency variation can be analysed.

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