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Performance Evaluation of Highly Efficient XOR and XOR-XNOR Topologies Using CNTFET for Nanocomputation

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Abstract: With excessive scaling in the VLSI industry, the Carbon Nanotube Field Effect Transistor(CNTFET) is emerging as a potential replacement to traditional MOSFET technology. XOR gate is an essential component in various digital logic circuit designs. Therefore it is crucial to devise a high performing XOR gate and XOR-XNOR gate to increase the overall efficiency of various XOR based digital circuits. This paper investigates the performance of several designs of individual XOR gates as well as simultaneous XOR-XNOR circuits for different applications. The implemented circuits have been analyzed and compared by parameters namely transistor count, delay, power dissipation, and power-delay product, and Energy delay product. The driving capability of the circuits has been verified for load capacitance of 2fF to 100fF. All circuits are simulated using Cadence Virtuoso Analog Environment in 45nm MOS technology and 10nm CNTFET model at 0.6-1.4V supply. The noise margin analysis of each XOR gate is also carried out. The most efficient topologies for individual XOR and XOR-XNOR circuits are found to be 97% more efficient than their counterparts. The layouts of the most efficient topologies have been implemented to calculate the circuit area. Monte Carlo simulation is done to establish the circuit's reliability. The implemented circuits perform remarkably better with a 10nm CNTFET model, thereby establishing emerging CNTFET technology as a promising replacement to MOSFET.

Keywords: CNTFET, XOR, XOR-XNOR, Low power, Montecarlo

1. Introduction

Digital circuit performance enhancement is possible through the implementation of the highly efficient precise logic gates [1], [2]. Logic gates like Inverter, NOR,NAND, and XOR are the most common building blocks of various digital circuits.XOR(Exclusive OR) gate is an essential component in various digital circuits like the full adder, half adder, parity generator, comparator, hybrid adder, and encryption processor [3]. Apart from that XOR gate is crucial to most cryptographic algorithms. The XOR gate is used as a Cipher because of its anti-coincident property, and the same architecture can be used for both encryption and decryption. As an important component in digital logic circuit design, the XOR gate provides a noteworthy contribution to the power expenditure and overall efficiency of the circuit. Thus to optimize digital circuits, it is necessary to use efficient XOR components in the circuit and boost the working of the circuit [4]. The continuous trend of scaling down VLSI technology has to lead to leakage and reliability problems such as elevated leakage current, short channel effect, interconnect problems, etc. CNTFET is an emerging alternative for traditional MOSFET devices [5]. The circuits implemented using CNTFET give advantages by their improved management over the device channel, short channel effects reduction, and lesser leakage current [6]. The XOR gate circuits implemented using CNTFET consume minimum power and energy [7], [8]. Thus an effort has been to implement some efficient XOR gates and XOR-XNOR gates in 10 nm CNTFET using the Stanford CNTFET model [9]. In this paper, several reportedly efficient topologies for the XOR gate and simultaneous XOR and XOR–XNOR gates are evaluated using both CNTFET and MOSFET to determine the most power-efficient circuits in this low power era. The implemented circuits have been analyzed and compared by transistor utilization, delay, power dissipation, Noise Margin, Power-Delay Product (PDP), and Energy Delay Product (EDP) by using Cadence Virtuoso Analog Design Environment. The paper's organization is as follows: The introduction to the paper is in Section 1, Section 2 discusses the structure and working of various individual XOR gates which are followed by a discussion on XOR-XNOR gates. It is followed by the simulation results in Section 3. The comparison and evaluation of all implemented topologies

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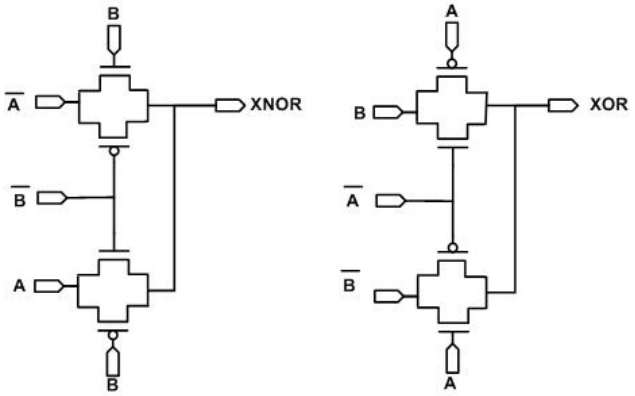

Figure 1. XOR gate and XNOR gate design using Transmission gates

are carried out in this section. To conclude, a conclusion is made in the last section 4.

2. Efficient XOR and XOR-XNOR Topologies

A. XOR Gate Topologies

Various high performing XOR topologies are proposed in the literature [3-4,10-13]. The most basic XOR gate available is standard CMOS based using Transmission gates, it has two inverters because complemented inputs are required by this design. The conventional topology of the XOR and XNOR gate based on the transmission gate is depicted in Figure 1 [10]. It operates with a great output voltage swing but in hindsight, it needs 12 transistors, which is a high transistor count compared to its counterparts.

VLSI industry is moving towards miniaturization and low power design. Several other designs have been proposed over time that utilizes comparatively lesser transistors and hence provides lower power dissipation. Thus this paper focuses on the reported efficient XOR circuits comprising of fewer transistors. Some topologies have the drawback of poor output signal level for some inputs but this can be solved by handling the W/L ratio till satisfactory output is obtained. The first implemented XOR circuit contains 4 transistors. This XOR gate comprises 2 PMOS and 2 NMOS is reported in the literature [10]. It has no DC supply.Figure.2(a) and2(b) show the 4-transistor topology of the XOR gate employing CMOS and CNTFET respectively. This structure shows some output degradation for certain inputs.

Another 4 transistors based XOR gate design [10]. This pass transistor based structure comprising of a DC power supply,2 PMOS, and 2 NMOS shown in Figure 3 must be faster than the circuit reported in Figure 2.Since this design is based on pass transistors some le1el loss is observed in the output for certain inputs. The output voltage level of the XOR gate illustrated in Figure 3 is enhanced even more by modifying the design with an additional standard inverter as an output driver to get a good output. Thus the total transistor count increases to 6 but the output voltage swing increases. Figure 4 shows the schematic for the 6T

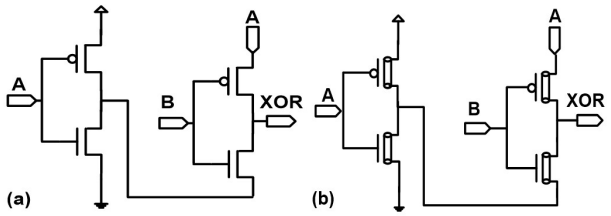

Figure 2. Inverter based XOR(a) Based on CMOS technology (b)Based on CNTFET technology.

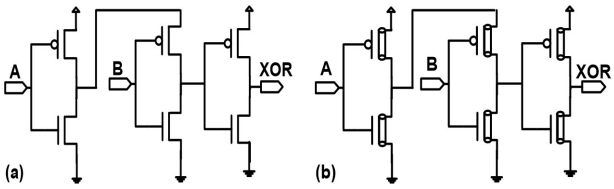

Figure 3. 6T XOR (a) Based on CMOS technology (b)Based on CNTFET technology.

XOR circuit [11]. 3 Transistors based XOR circuit has been reported in research [12], [13]. It consists of 2 PMOS and 1 NMOS. This structure again shows voltage degradation at the output for a certain input, which can be fixed by W/L manipulated to get better output. The schematic is shown in Figure 5. Finally, a seven transistor-based XOR circuit was proposed by Naseri et al. in 2018. This circuit is supposed to perform efficiently despite increased transistor count and it provides a full swing as well [4]. All five individual XOR gates with low transistor count are implemented and analyzed in Cadence Virtuoso at 45nm MOSFET and 10nm CNTFET technology.

B. Simultaneous XOR-XNOR gates

Hybrid adders, approximate adders, and multipliers, etc are some of the many applications of simultaneous XOR-XNOR in digital circuits. Several XOR-XNOR topologies have been reported in [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27] out of which some of the best performing circuits are implemented in this paper. First, a double pass transistor logic (DPL) based XOR-XNOR is implemented. The total transistor count comes to be 12 including the two inverters employed to generate the complemented output of both the inputs. Figure 7 shows the aforementioned DPL XOR-XNOR gate circuit [14]. This circuit is said to provide full swing but delay and power

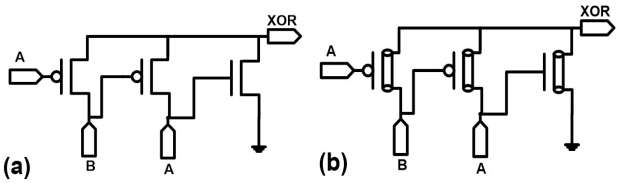

Figure 4. 3T XOR (a) Based on CMOS technology (b)Based on CNTFET technology.

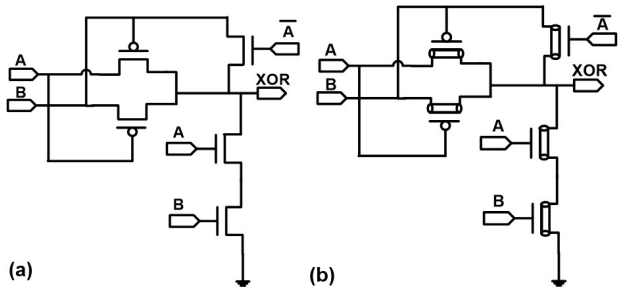

Figure 5. 7T XOR (a) Based on CMOS technology (b)Based on CNTFET technology.

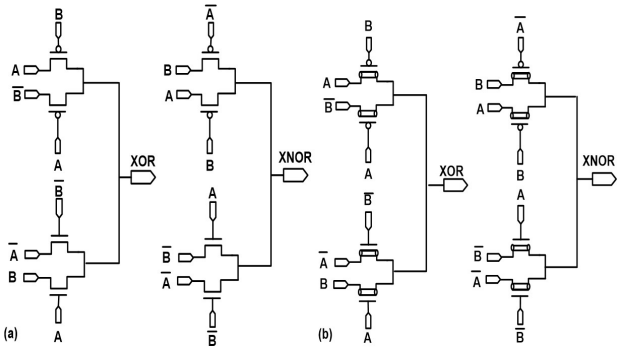

Figure 6. DPL based XOR (a) Based on CMOS technology (b)Based on CNTFET technology.

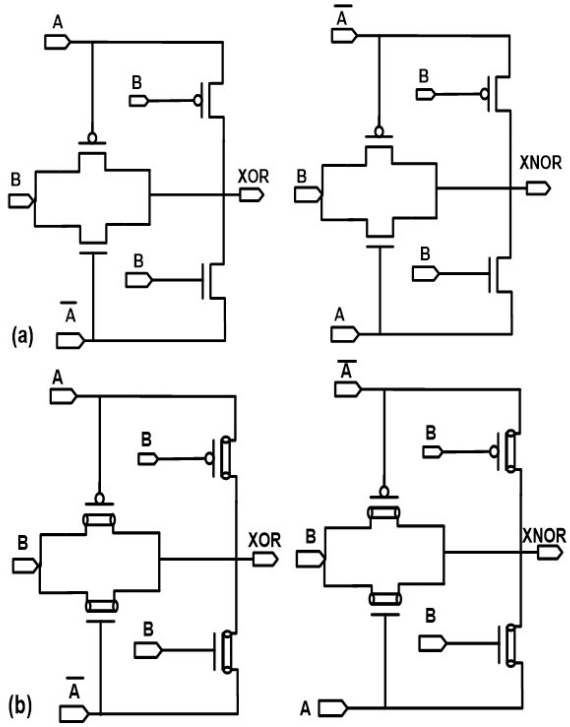

Figure 7. PTL based XOR (a) Based on CMOS technology (b)Based on CNTFET technology.

dissipation are affected because of the presence of two power intense inverters.

Figure 8 shows the XOR-XNOR gate based on Pass transistor logic [3], which is implemented by employing 10 transistors. Theoretically, the PTL logic style is better than the DPL logic style. Compared to the DPL based XOR-XNOR the transistor count is reduced by two.

Several other structures for XOR-XNOR provide simultaneous output for both XOR and XNOR outputs. Since glitches can be avoided by utilizing simultaneous signals having the same delay, therefore they are preferred for the implementation of hybrid adders. Figure 9 depicts a CPL logic based XOR-XNOR circuit based on CPL logic [14]. Total transistors employed in this circuit are 10 including the two inverters for complemented inputs.

The working of CPL based simultaneous XOR-XNOR was improved in [15] by removing an inverter to bring down the circuit's power dissipation. Figure 10 shows improved CPL based simultaneous XOR-XNOR circuits having 8 transistors.

Figure 11 shows a simultaneous XOR-XNOR circuit having just six transistors [16]. It employs two complementary transistors (PMOS and NMOS) to restore the output voltage level which is affected due to degradation.

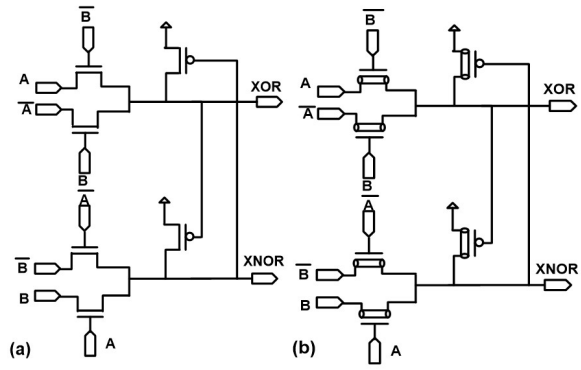

Figure 8. CPL based XOR-XNOR 1 (a) Based on CMOS technology (b)Based on CNTFET technology.

An improved version of 6T simultaneous XOR-XNOR is given in Chang et al. in 2005. It improves the response of the circuit and output swing. This circuit consists of four extra transistors compared to the previous design, thus bringing the total transistor count up to 10 transistors [17]. These extra transistors improve the swing at the expense of increased power.10T simultaneous XOR-XNOR circuits using CMOS and CNTFET are depicted in Figure 12.

Another improvement of the structure of simultaneous 6T XOR-XNOR is shown in Figure 13 [18]. In this

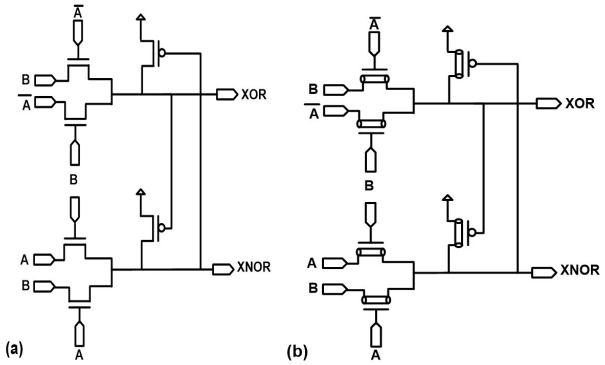

Figure 9. CPL based XOR-XNOR 2(a) Based on CMOS technology (b)Based on CNTFET technology

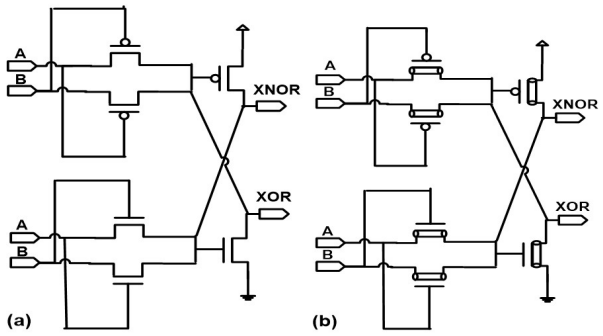

Figure 10. 6T XOR-XNOR 2(a) Based on CMOS technology (b)Based on CNTFET technology

topology, one input is complemented by an inverter circuit and two level restoring transistors (one PMOS and one NMOS) are added.

Figure. 14 shows the 8T XOR-XNOR [19] circuit which was given by Wang et al. This circuit's performance is satisfactory with respect to delay and power dissipation but output voltage swing degrades for one input combination.

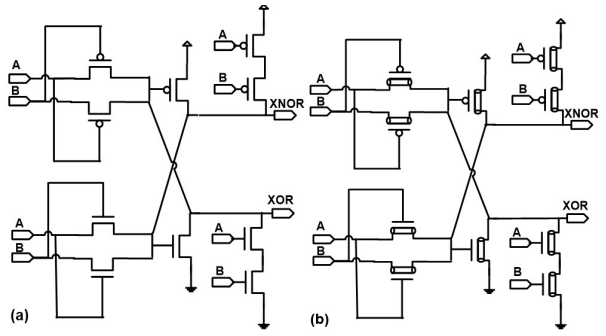

Figure 11. 10T XOR-XNOR 1(a) Based on CMOS technology (b)Based on CNTFET technology

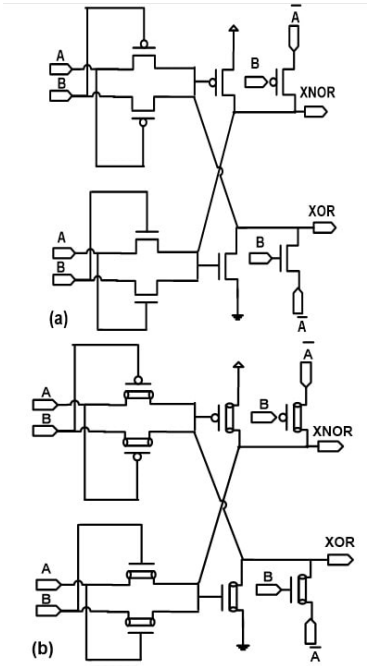

Figure 12. 10T XOR-XNOR 2(a) Based on CMOS technology (b)Based on CNTFET technology

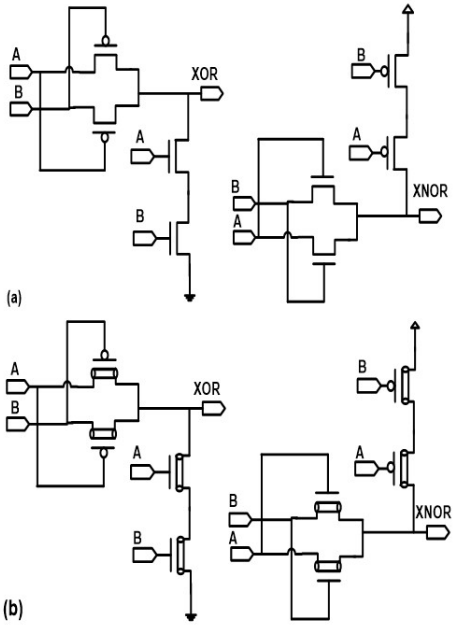

Figure 13. 8T XOR-XNOR (a) Based on CMOS technology (b)Based on CNTFET technology

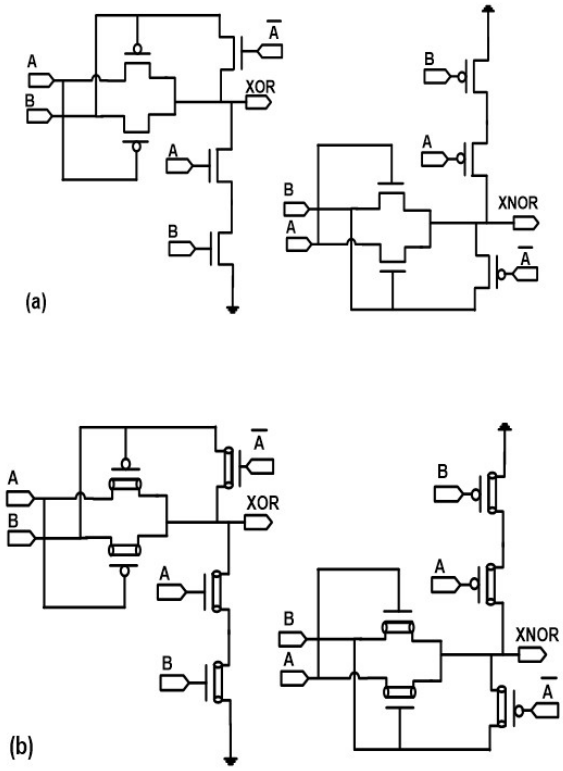

Figure 14. 12T XOR-XNOR (a) Based on CMOS technology (b)Based on CNTFET technology

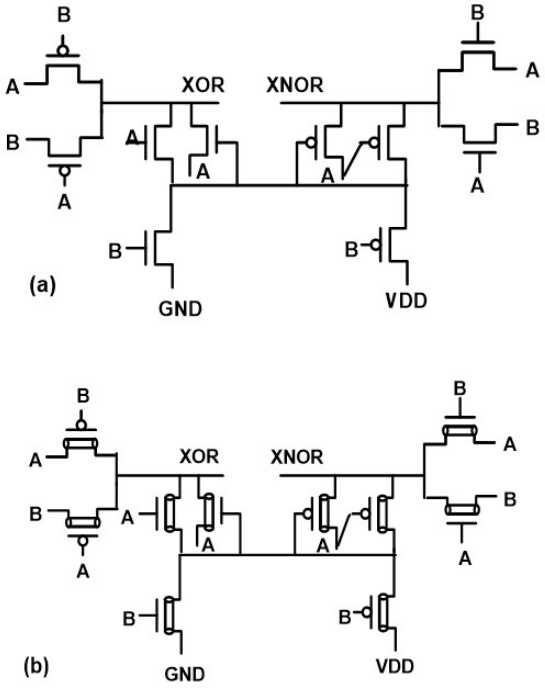

Figure 15. 10T XOR-XNOR 3 (a) Based on CMOS technology (b)Based on CNTFET technology

This drawback of voltage degradation was removed by Naseri et al in 2018. They proposed a 12T XOR-XNOR which overcomes the drawbacks of the 8T XOR-XNOR circuit [4]. The 12T XOR-XNOR circuit is depicted in Figure 15.

10T XOR-XNOR 3 circuit depicted in Figure 16 is an improvement over 12T XOR XNOR as the external NOT gate present in the above circuit was removed by Kandpal et al. [20]. Thus transistor count is reduced by two.

The scaling of CMOS as per Moore's Law is reaching its saturation as transistor channel length reaches a lower nanometer range, which has lead to degradation in the performance of transistors and hence the circuits [28]. It is found that reducing channel length beyond 45nm exponentially increases leakage current. CNTFET is touted as a potential replacement for CMOS through wide research. Amid other emerging technologies CNTFETs are popular due to their exceptional physical and electrical properties which include better channel control, high electron mobility and current density, increase in transconductance, etc. Apart from that fabrications of CNTFETs are similar to that of regular CMOS. And various studies have established that CNTFET based circuits provide better performance in comparison to CMOS-based circuits. Hence this emerging nanotechnology is a powerful alternative to CMOS. Researchers have proved that CNTFET based circuits are better performing than CMOS-based circuits [29], [30]. Hence all aforementioned circuits are implemented using the 10nm Stanford CNTFET model and their schematic is shown as Figure(b) in every circuit above. These implemented circuits are compared with their CMOS-based counterparts to establish their superior performance.

3. Results and Discussions

All implemented individual XOR gates and different simultaneous XOR-XNOR designs are analyzed for their transistor count, power, delay, PDP, Noise Margin, and EDP. For a fair comparison, each topology is analyzed under the same conditions to calculate all the parameters. The transient and DC analysis of each topology is done at a supply voltage range of 0.6V- 1.4V utilizing 45nm gpdk technology for 200ns. Most optimum circuits were implemented using the 10nm CNTFET Stanford Model and their corner analysis is done as well. Parameter analysis by Voltage variation is also done for all circuits for the range of 0.6V- 1.4V. Figure 17 shows the general transient response of individual XOR gate and XOR-XNOR gate respectively.

A. XOR Results and Analysis

First, Table 1 summarizes the findings of individual XOR gates. The latency , average power dissipation, PDP, and EDP of the XOR gates, as well as transistor utilization count in the circuits.

From Table 1 it can be inferred that Inverter based XOR circuit is providing the best performance in terms of min-

TABLE I. XOR circuits parameters

Design	Transistors	Average power (uW)	Delay(fs)	PDP(aJ)	EDP(Js)
6T XOR	6	0.0865	21910	1.90	4.15×10^{-29}
Inverter based XOR	4	0.0604	29.97	0.0018	5.429×10^{-35}
4T XOR	4	9.62	180.9	1.74	3.15×10^{-31}
3T XOR	3	6.57	215.5	1.41	3.04×10^{-31}
7T XOR	7	9.81	346.9	3.40	1.18×10^{-30}

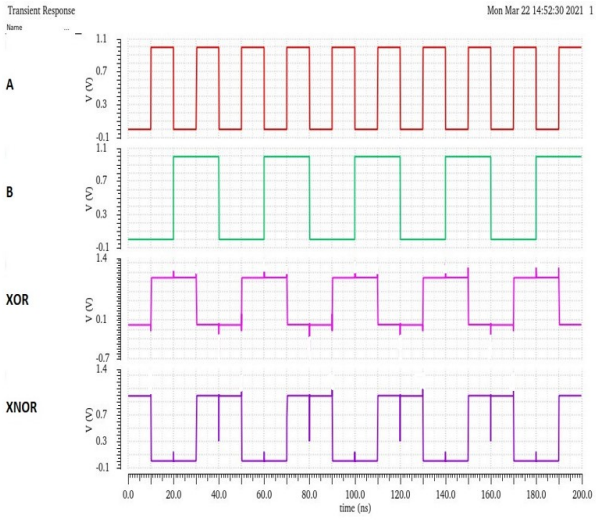

Figure 16. Transient Response of XOR-XNOR gates

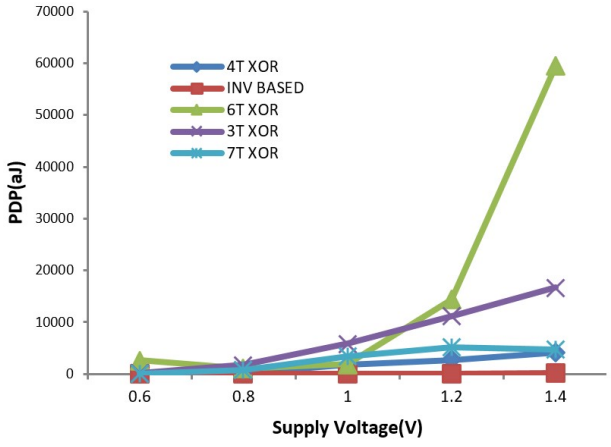

Figure 17. PDP variation with respect to voltage for all implemented XOR CMOS based gates.

imum power dissipation, PDP, and EDP.PDP improvement is upto upto 97% .Figure 18 summarizes the results of PDP variation with respect to the Supply voltage. From the trends, it is evident that inverter-based XOR is giving the least power dissipation for all conditions.

To calculate the PDP plotted in Figure 18, each XOR

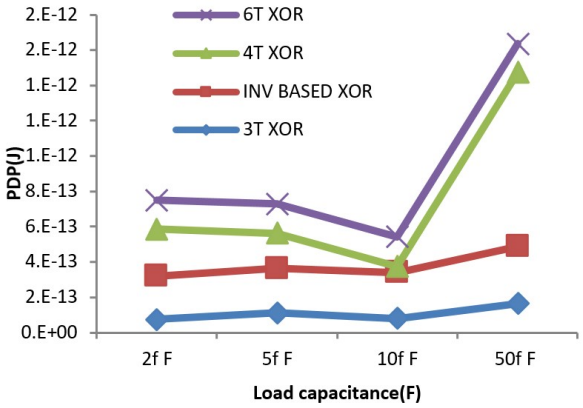

Figure 18. Load analysis of implemented individual XOR gates

gate was analyzed at different voltages from 0.6 to 1.4V. Table 2 and 3 contains the power and delay observed of all individual gates with respect to supply voltage variation from 0.6V to 1.4V. Table 2 contains the power and delay observed of all individual gates with respect to supply voltage variation from 0.6V to 1.4V.

Now, the Noise margin is calculated for all the individual XOR circuits from their DC analysis as shown in Table 4. Noise Margin is the ability of a certain circuit to tolerate noise and it has been calculated using the following formula- N ML = VIL – VOL (1) NMH = VOH – VIH (2) Where NML and NMH are low noise margin and high noise margin respectively.

The inverter-based XOR appears to have the optimum results in terms of PDP and EDP based on simulation outcomes. Around 97% improvement in PDP is observed.

All individual XOR gates are analyzed over a range of load capacitance of 2fF to 50fF. The PDP of each gate is plotted in Figure 19. The PDP of the 7T XOR gate is very high(in the range of 10^{-11})hence it is not included in this graph. It is consistently observed that 3T XOR and Inverter based XOR is showing the least PDP in each case, which confirms its optimum performance. Hence process variation analysis of Inverter-based XOR is done as well in order to establish its functionality. The results obtained are included

TABLE II. Individual XOR gate power dissipation(uW) with respect to supply voltage variation

Supply voltage (V)	4T XOR	INV XOR	6T XOR	3T XOR	7T XOR
0.6	0.0072	0.008	0.012	0.71	0.0145
0.8	1.35	0.039	0.023	9.26	1.47
1	9.62	0.08	0.086	38.96	9.81
1.2	23.55	0.218	0.98	89.08	23.76
1.4	42.14	1.057	5.45	158.62	42.92

TABLE III. Individual XOR gate delay(fs) with respect to supply voltage variation

Supply voltage (V)	4T XOR	INV XOR	6T XOR	3T XOR	7T XOR
0.6	229.9	353.24	219050	235.88	316.8
0.8	173.2	188.76	44190	187.2	500
1	180.9	150.5	21910	150.97	346.9
1.2	114.9	246.86	14690	125.3	216.36
1.4	97.15	212.14	10900	105.3	110.8

TABLE IV. Noise Margin of individual XOR circuits

Individual XOR design	VOH (V)	VIH (V)	VIL (V)	VOL (V)	NML (V)	NMH (V)
Inverter based XOR	1	0.66	0.33	0	0.33	0.34
6T XOR	1	1	0	0	0.1	0.1
4T XOR	1	0.8	0.2	0	0.2	0.2
3T XOR	1	0.83	0.23	0	0.23	0.17
7T XOR	1	0.7	0.17	0	0.17	0.3

TABLE V. Process corners of inverter based XOR

Corners	Avg power (uW)	Delay (fs)	PDP (aJ)	EDP (Js)
TT	9.63	119.34	1.14	1.3×10^{-31}
FF	12.22	20.16	0.24	4.8×10^{-31}
SS	7.21	212.8	1.5	3.19×10^{-31}
FS	10.68	97.74	1.04	1.01×10^{-31}
SF	8.49	62.42	0.53	0.33×10^{-31}

in Table 5.

By process corner variation the min and max value of average power of the circuit is 7.21uW and 12.22uW respectively. Similarly, Min and max values of delay observed by process corners are 20.16fs and 212.8fs respectively. After establishing an Inverter Based XOR structure having four transistors as the superior individual XOR design compared to its current counterparts. The same circuit when implemented using 10nm CNTFET where 68% improvement in PDP improvement is observed at 1V supply. Their delay, power dissipation, and PDP are calculated at different supply voltages is calculated and it is found that CNTFET based circuit is consistently superior performing than the CMOS-based circuit as seen in Figure 20 and Table 6.

TABLE VI. Comparison of parameters of Inverter based XOR implementation using CMOS and CNTFET

Supply Voltage (V)	CMOS			CNTFET		
	Power (uW)	Delay (fs)	PDP (zJ)	Power (uW)	Delay (fs)	PDP (zJ)
0.6	0.0127	8280	105.81	0.008	353.24	2.82
0.8	0.019	1839	34.86	0.039	188.76	7.36
1	0.084	463.4	38.925	0.08	150.5	12.04
1.2	4.85	393.9	1910	0.218	246.86	53.815
1.4	17.36	341.3	5924	1.057	212.14	224.23

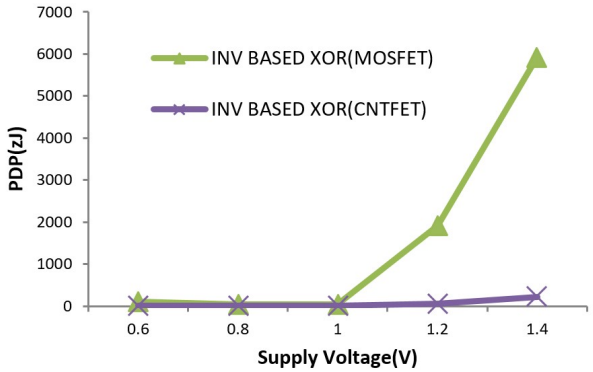

Figure 19. PDP comparison of inverter-based XOR using CMOS and Inverter based XOR using CNTFET.

From Figure 20 it is quite clear that CNTFET based circuit gives superior performance than CMOS based circuits with 68-96%improvement in PDP.

Monte Carlo simulation of the power dissipation by inverter based XOR is done by using 200 samples. The results indicate that the mean value is 58.814nW and the standard deviation is 7.39nW as seen in figure 21.

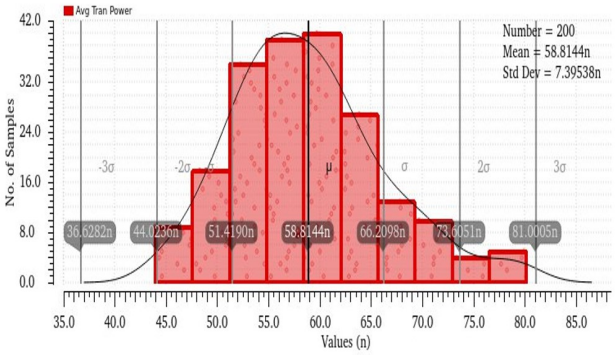

Figure 20. Monte Carlo Simulation of power dissipation by Inverter based XOR using 200 samples.

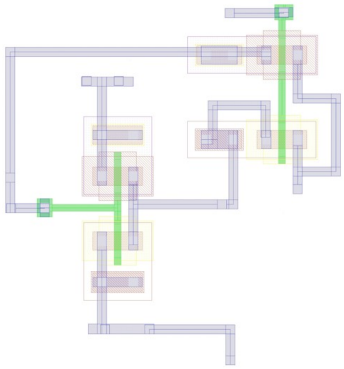

Figure 21. The layout of Inverter based XOR.

From the implemented layout as seen in Figure 22, the area occupied by the Inverter-based XOR XNOR circuit using 45 nm gdpk comes to be 6.923 um^2.

B. Simultaneous XOR-XNOR Results

The XOR-XNOR designs are also extensively analyzed over the same simulation setup. Table 7 summarizes the transistor count, average power, delay, PDP, and EDP of the XOR-XNOR topologies.

From the analyses, 10T XOR XNOR 3 is showing the best performance as its PDP is 68.3–99% better than other circuits. Table 8 shows the Noise margin of all the discussed circuits. From the table, it can be inferred that the noise margin is of an acceptable level. Apart from that the driving capability of all these gates has been tested over a capacitive load of 2fF to 100fF. All the circuits are analyzed over the supply voltage variation from 0.6V to 1.4V. Figure 23 depicts the variation of average power dissipation with supply voltage variation.

Figure 24 and Figure 25 shows the change of Delay and PDP with respect to Supply Voltage variation respectively. In all cases, the 10T XOR-XNOR 3 circuit is showing the best performance.

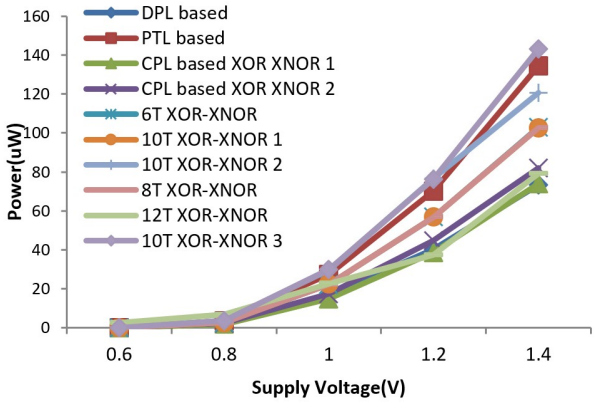

Figure 22. Power(uW) of XOR XNOR gates with respect to Supply Voltage variation.

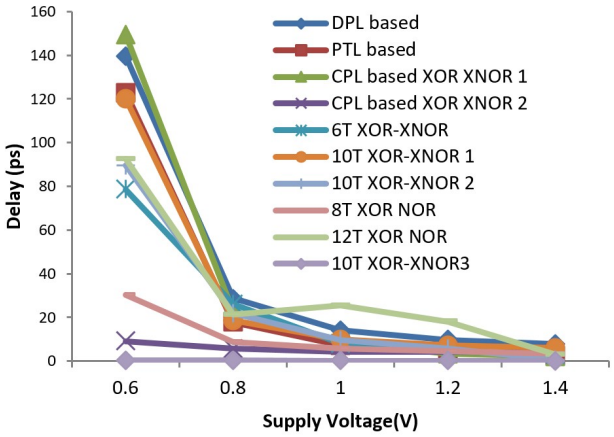

Figure 23. Delay(ps) of XOR XNOR gates with respect to Supply Voltage variation.

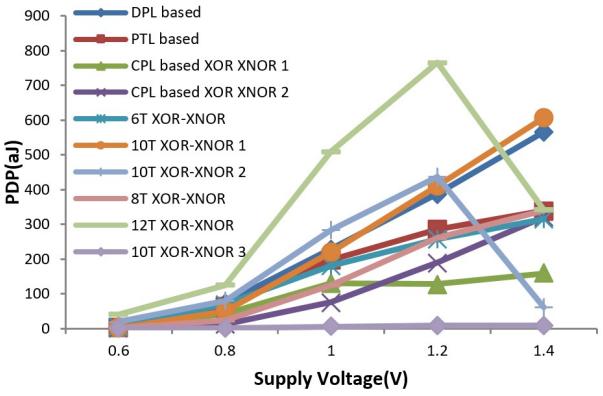

Figure 24. PDP of XOR XNOR gates with respect to Supply Voltage variation.

TABLE VII. CMOS based XOR-XNOR design comparison

Design	No. of trs.	Average Power(uW)	Delay (ps)	PDP (aJ)	EDP ($10^{-30}Js$)
DPL based XOR- XNOR	12	16.33	14	228.62	3200.6
PTL based XOR XNOR	10	26.7	7.2	192.24	1384.1
CPL based XOR XNOR 1	10	11.96	16	191.36	3061.7
CPL based XOR-XNOR 2	8	14.73	1.18	17.381	20.51
6T XOR-XNOR	6	15.63	47.88	748.364	35832
10T XOR-XNOR 1	10	22.33	9.8	218.83	2144.5
10T XOR-XNOR 2	10	29.83	9.53	284.27	2709.1
8T XOR-XNOR	8	22.3	5	111.5	557.5
12T XOR-XNOR	12	28.3	6	169.8	1018.8
10T XOR-XNOR 3	10	29.9	0.1842	5.506	1.014

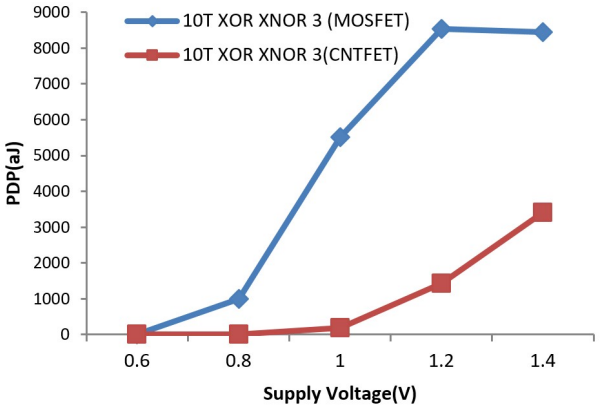

Figure 25. PDP variation of CPL based XNOR XNOR 2 circuit using CMOS and CNTFET with respect to supply voltage variation

The Noise Margin of implemented XOR-XNOR circuits is tabulated in Table 8 which shows each gate has an acceptable level of noise margin.

From all the XOR-XNOR, 10T XOR XNOR 3 topology depicts the most superior performance hence its process variation is also done and the results obtained are summarized in Table 9. By process corner variation the min and max value of average power of the circuit is 22.89uW and 30.135uW respectively. Similarly, Min and max values of delay observed by process corners are 74.42fs and 89.09fs respectively. The same circuit is implemented using CNTFET and it is observed that there is an improvement in PDP by 78% at 1V supply voltage. Again the parameters for both CMOS based circuit and CNTFET based circuit are observed under voltage variation of 0.6V to 1.4V and the Table 10 lists the results obtained.

The CNTFET based implementation of 10T XOR XNOR 3 shows substantial performance improvement from 30%- 98% in power delay product.

As per the trends of Figure 26, CNTFET based 10T XOR XNOR 3 circuit shows optimum performance with respect to CMOS based structure.

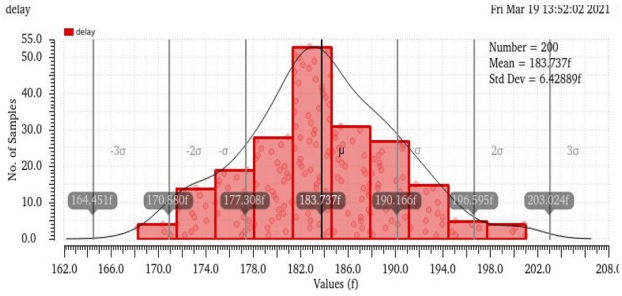

Figure 26. Monte-Carlo simulation of worst-case delay of 10T XOR-XNOR 3

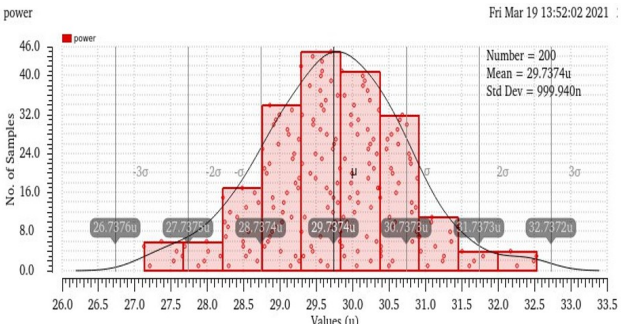

Figure 27. Monte-Carlo simulation of average power dissipation of 10T XOR-XNOR 3

Figure 27 shows the Montecarlo simulation of delay of 10T XOR XNOR 3 having a 200 sample count. From there we can infer that the mean delay is 180.73fs with a standard deviation of 6.42fs.

Figure 28 shows the Montecarlo simulation of Power dissipation by 10T XOR XNOR 3 having a 200 sample count. From there we can infer that the mean power is 29.737uW with a standard deviation of 999.94nW.

From the implemented layout as seen in Figure 29, the area occupied by the 10T XOR XNOR 3 circuit using 45 nm gdpk comes to be 22.59 um^2.

TABLE VIII. Noise margin(V) of XOR-XNOR circuits

XOR- XNOR CIRCUITS	VOH (V)	VIH (V)	VIL (V)	VOL (V)	NML (V)	NMH (V)
DPL based XOR- XNOR	0.85	0.78	0.05	0	0.05	0.07
PTL based XOR-XNOR	0.86	0.76	0.18	0.06	0.12	0.1
CPL based XOR-XNOR 1	1	0.81	0.19	0	0.19	0.19
CPL based XOR-XNOR 2	1	0.85	0.19	0	0.19	0.15
6T XOR-XNOR	1	0.8	0.177	0	0.177	0.2
10T XOR-XNOR 1	1	0.8	0.18	0	0.18	0.2
10T XOR-XNOR 2	0.95	0.79	0.1	0.04	0.06	0.16
8T XOR-NOR	1	0.78	0.17	0	0.17	0.22
12T XOR-NOR	1	0.79	0.43	0	0.43	0.21
10T XOR-XNOR 3	1	0.79	0.12	0	0.12	0.21

TABLE IX. Process corners of 10T XOR-XNOR circuit

Process corners	Avg Power (uW)	Delay (fs)	PDP ($10^{-21}J$)	EDP ($10^{-18}Js$)
TT	29.94	80.28	2403.5	192.95
FF	30.04	80.61	2421.5	195.19
SS	22.89	82.91	1897.8	157.34
FS	30.135	74.2	2236	165.91
SF	29.029	89.09	2586.2	230.40

TABLE X. Parametric comparison of implementation of 10T XOR-XNOR 3 using CMOS and CNTFET

Supply (V)	CMOS			CNTFET		
	Avg Power (uW)	Delay (fs)	PDP (10^{-20} J)	Avg Power (uW)	Delay (fs)	PDP (10^{-20} J)
0.6	0.02	336	0.8	0.02	335.7	0.5
0.8	3.58	276	99.1	3.58	276.5	1.0
1	29.8	184	550	29.89	184.2	18.7
1.2	76.2	112	854	76.21	112.1	143
1.4	143	59	845	143	59.05	340

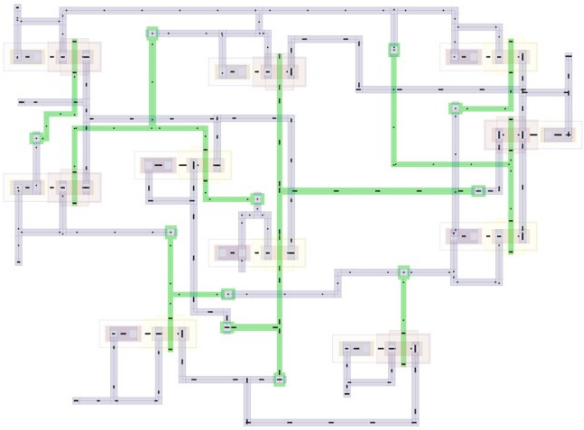

Figure 28. The layout of 10T XOR XNOR using 45nm gdpk

4. Conclusion

In this paper, various high performing designs of individual XOR gates and XOR-XNOR gates have been implemented and their performance parameters have been evaluated in order to determine the most efficient structures for digital applications. These circuits are simulated and analyzed over various performance parameters viz Power dissipated, delay, PDP , EDP, driving capability , Noise Margin Analysis and transistor count at various supply voltages. Apart from that Monte Carlo simulation of the best performing circuit has been done to show the feasibility of the circuits. All parameters are observed at a supply voltage variation of 0.6V to 1.4V. The driving capability of individual XOR circuits has been investigated for the load capacitor of 2fF to 100fF at 1 V supply voltage. Cadence Virtuoso is used for all the simulations at 45 nm technology and 10nm Stanford CNTFET model. The Inverter based XOR circuit is depicting the best performance using 4 transistors in individual XOR circuits and hence its deemed as the most efficient compared to others as it shows an improvement of around 97%. In XOR-XNOR circuits With high speed, decreased power consumption, and a reasonable signal level for all input combinations, the 10T XOR XNOR 3 gate achieves the lowest PDP(68.3-99%).Their CNTFET-based circuits outperform their CMOS-based counterparts by 31 to 98percent, proving CNTFET as a potential alternative to conventional MOSFETs.

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