



Performance Analysis of a High-Throughput LDPC Decoder Using Sum Product and Min Sum Algorithm

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Abstract: This paper presents Verilog implementation of Low-Density Parity-Check (LDPC) decoders using Sum-Product and Min-Sum algorithms which will take more area as compared to other decoding algorithms. In this paper, area efficient LDPC decoder depending upon abridged complexity Minsum algorithm is presented. It reduces the permutational complexity with limiting the extrinsic information bit length to 4 bits and it modifies the check and variable node processing operation. Compilation at an algorithmic level explains that the proposed decoder attain good error performance as compared to a Sum Product Algorithm based decoder, and consequently handles the problem of immense error performance deprivation of a LDPC decoder. A Min Sum Based LDPC decoder with a matrix length (1000, 500) has been implemented in a MATLAB with a 10^{-1} BER and the design is implemented in HDL Verilog. The complete top level module was done by structural modeling style and simulated with SPARTAN FPGA Family. The percentage saving in area is about 33% of slices and provides a throughput of 1.46Gbps.

Keywords: Message Passing Algorithm, Area, Slices, LDPC Decoder, Throughput.

1. INTRODUCTION

Standard communication systems such as wireless communication, memory require very fast forward error correcting schemes. The close to Shannon limit performance of LDPC codes [1] algorithms namely sum product [2], min-sum, and modified min-sum [3], has helped LDPC codes to be useful in various systems such as Wireless applications, Wi-Fi, 10Gbit Ethernet and others. However, due to exponential functions implicated in their algorithms, LDPC decoders are frequently ignored due to bulky storage requirement. Parallel architectures frequently result in large area overhead, whereas serial architectures are very sluggish for many applications. As far as memory requirements are concerned, rate of the code and block length is also significant. With the enhancements in deep ULSI procedures, different block length and rate flexible LDPC decoders have been presented [7-8].

This paper is organized as follows. Section II introduces the previous work done related to sum product and min sum algorithm. In section III, message-passing algorithm is described. Section IV presents numerical results and analysis of this LDPC Decoder and summarizes the conclusion for area resources and

compares the results with other decoder architectures. Conclusions are outlined in Section V.

2. PREVIOUS WORK

In new era, Low-Density Parity-Check has engrossed significant attention because of its performance closed to Shannon boundary. The low-density parity-check codes [1] can be decoded using various message passing methods namely soft and hard-decision methods. The soft-decision based decoding algorithms, such as sum product (SP) algorithm and min-sum (MS) algorithm [2], can attain exceptional recital but frequently with intense computational complexity. As the speed of electronic systems increases, it became practical to adopt the computationally expensive but powerful LDPC codes in the fibre-optic communication systems [3-4].

A. Decisions: Hard Versus Soft

The standard communication system consists of Source encoder, Channel and source decoder. The noise will appear because the channel is wired or wireless. The same system is as shown in figure 1. There are various iterative decoding algorithms for LDPC decoder.

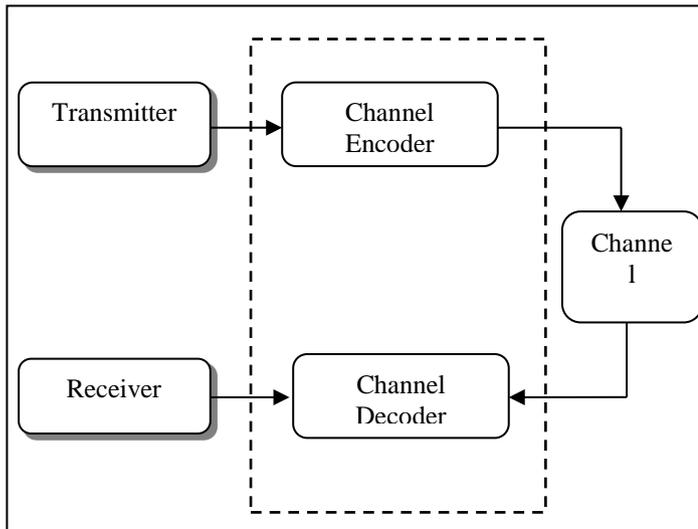


Figure 1. The Standard Communication System

They are based on the decisions to be taken for decoding the techniques used. They are categorized into hard and soft decision decoding respectively. They are again categorized with respect to their numerical complexities to be decoded for diverse channel codes. In hard decision scheme, first the odd or even parity will be decided by checking errors in bits and then information bits are sending from variable to check nodes. And then If number of 1's received at check nodes satisfies the required parity, then it sends the same data back to message node, else it adjusts each bit in the received data stream to satisfy the required parity and then transmits the new message back to message nodes. Therefore, in every case, check node received the bits from variable node and done the calculation for the information bits and also checked whether the parity check equations are satisfied or not. The decoding method will continue till all the parity check equations are satisfied. The hard decision and soft decision is as shown in Figure 2. The message-passing algorithms are also known as iterative decoding algorithms as the messages pass forth and backward direction between the bit nodes and check nodes iteratively until a correct result is obtained. The other criterion is to give maximum iteration limit in an algorithm. If the algorithm execution reaches the given iteration limit then the operation will stop and shows the decoded codeword's. Depending on the frames given in the MATLAB program, execution will take more time.

For functional checking of the code, initially fewer frames can be given on order to reduce the execution time.

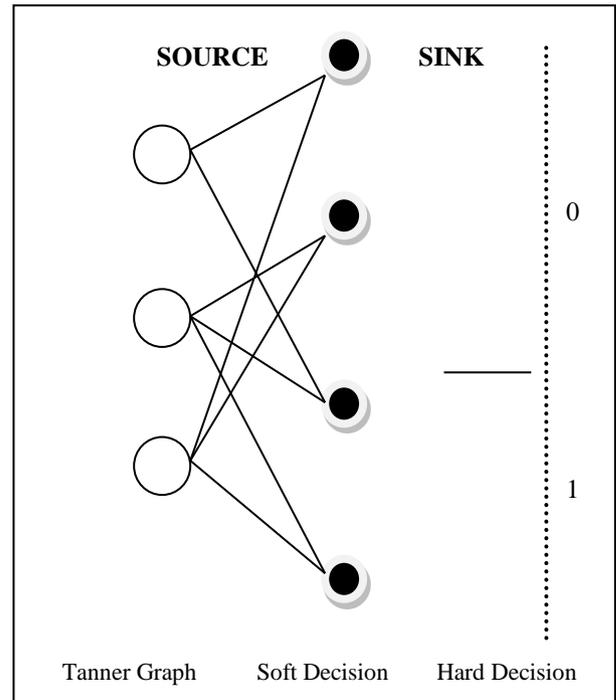


Figure 2. Soft Decision Vs Hard Decision

3. LDPC DECODING ALGORITHM

3.1 Sum Product Algorithm in Log Domain

Message passing algorithms finds the heart in LDPC Decoder. These algorithms are using Tanner graphs to represent the cyclic graphs. The bits or information passing decoding algorithms used to decode LDPC codes are collectively termed message-passing algorithms since their operation can be solved giving a detailed description by the passing of messages in terms of bits all along the edges of a Tanner graph. Each Tanner graph node works in segregation, only having access to the information contained in the messages on the edges connected to it.

$$H = \begin{bmatrix} 1 & 1 & 0 & 1 & 0 & 0 \\ 1 & 0 & 1 & 0 & 1 & 0 \\ 0 & 1 & 1 & 0 & 0 & 1 \\ 0 & 0 & 0 & 1 & 1 & 1 \end{bmatrix}$$

Figure 3 shows the Tanner Graph for H Matrix. Various message-passing algorithms are named for the type of information's conceded at the nodes. Each algorithm has its own speciality.

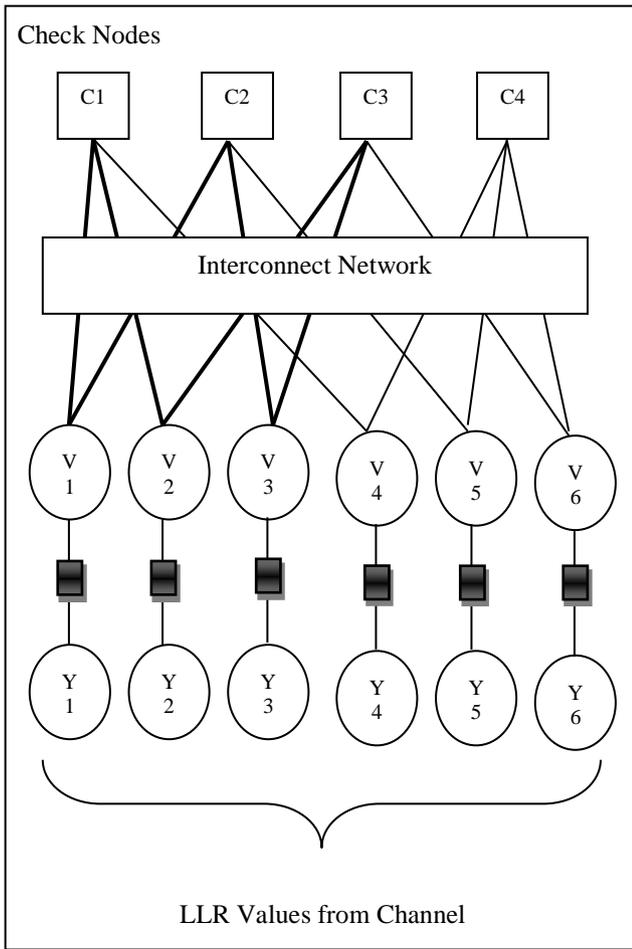


Figure 3. Tanner Graph for H Matrix

It is very expedient to signify probability values as maximum log likelihood ratios and when this is done through BP decoding is often called sum-product decoding algorithm since the use of log likelihood ratios allows the calculations at the bit and check nodes to be computed using sum and product equations.

Each variable node updates its decision depending upon the output and the extrinsic information received from all the neighbouring check nodes. In order to get the correct codeword, finally an intrinsic and extrinsic information codeword is added. The whole mathematical analysis is explained as shown in next section. Flowchart of the Algorithm is as shown in Figure 4.

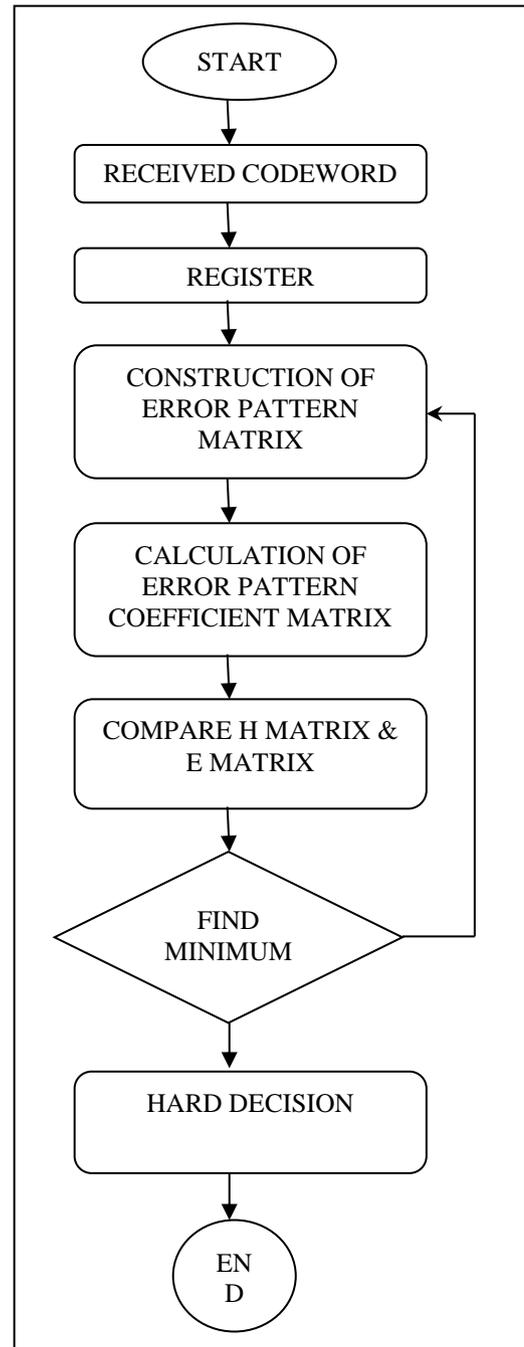


Figure 4. Flow chart of Algorithm



3.2. Mathematical Analysis of Sum Product Algorithm in Log Domain:

Let the Transmitted Codeword is $C = [0\ 0\ 1\ 0\ 1\ 1]$.

This codeword is transmitted over noisy channel and the received codeword is $Y = [1\ 0\ 1\ 0\ 1\ 1]$.

Step 1: Prior Probabilities for Binary Symmetric Channel are as follows.

$$H = \begin{bmatrix} 1 & 1 & 0 & 1 & 0 & 0 \\ 0 & 1 & 1 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 1 & 1 & 0 & 1 \end{bmatrix}$$

$$R_i = \log\left(\frac{1-p}{p}\right) \quad \text{if } Y_i = 0 \quad \text{-----} \quad (1)$$

For Binary Symmetric Channel, Let us consider $p = 0.4$, we have,

$$\log\left(\frac{p}{1-p}\right) = \log\left(\frac{0.4}{1-0.4}\right) = \log\left(\frac{0.4}{0.6}\right) = -1.0986 \text{ and}$$

$$\log\left(\frac{1-p}{p}\right) = \log\left(\frac{1-0.4}{0.4}\right) = \log\left(\frac{0.6}{0.4}\right) = +1.0986$$

Therefore, the Prior Log Likelihood Ratios are $R = [-1.0986, 1.09863, -1.09863, 1.09863, -1.0986, -1.0986]$

These are the intrinsic information probability values. These values are added to extrinsic information probability in order to get the corrected codeword.

Step 2: Horizontal Step: Calculation of M Matrix (Check Node Processing) From the below Table I, one can calculate the M Matrix that will be useful for calculation of Error Pattern Matrix.

TABLE I. CALCULATIONS OF M MATRIX

Column	M	From R Matrix	Values	M	From R Matrix	Values
Row	$M_{j,i}$	R_i		$M_{j,i}$	R_i	
i						
1	$M_{1,1}$	R1	-1.0986	$M_{3,1}$	R1	-1.0986
2	$M_{1,2}$	R2	+1.0986	$M_{2,2}$	R2	+1.0986
3	$M_{2,3}$	R3	-1.0986	$M_{4,3}$	R3	-1.0986
4	$M_{1,4}$	R4	+1.0986	$M_{4,4}$	R4	+1.0986
5	$M_{2,5}$	R5	-1.0986	$M_{3,5}$	R5	-1.0986
6	$M_{3,6}$	R6	-1.0986	$M_{4,6}$	R6	-1.0986

$$M = \begin{bmatrix} M_{1,1} & M_{1,2} & M_{1,3} & M_{1,4} & M_{1,5} & M_{1,6} \\ M_{2,1} & M_{2,2} & M_{2,3} & M_{2,4} & M_{2,5} & M_{2,6} \\ M_{3,1} & M_{3,2} & M_{3,3} & M_{3,4} & M_{3,5} & M_{3,6} \\ M_{4,1} & M_{4,2} & M_{4,3} & M_{4,4} & M_{4,5} & M_{4,6} \end{bmatrix}$$

$$M = \begin{bmatrix} -1.0986 & +1.0986 & -- & +1.0986 & -- & -- \\ -- & +1.0986 & -1.0986 & -- & -1.0986 & -- \\ -1.0986 & -- & -- & -- & -1.0986 & -1.0986 \\ -- & -- & -1.0986 & +1.0986 & -- & -1.0986 \end{bmatrix}$$

Step 3: Vertical Step: Calculation of Extrinsic Information Matrix- (Posteriori Information)

The prime logic for calculation of E matrix is that one has to exclude the error coefficient in that particular row. Calculation of error pattern matrix is as shown in table II.

TABLE II. LOGIC FOR CALCULATION OF ERROR PATTERN MATRIX

Calculation of Error Pattern Matrix				
Columns		J	j	j
Rows	i			
Check Task-1	1	1	2	4
Check Task-2	2	2	3	5
Check Task-3	3	1	5	6
Check Task-4	4	3	4	6

$$E_{j,i} = \log\left(\frac{1 + \prod_{i' \in \beta_j, i' \neq i} \tanh(M_{j,i'} / 2)}{1 - \prod_{i' \in \beta_j, i' \neq i} \tanh(M_{j,i'} / 2)}\right) \quad \text{-----} \quad (2)$$

$$E = \begin{bmatrix} 9.2098 & -9.2098 & --- & -9.2098 & --- & --- \\ --- & 9.2098 & -9.2098 & --- & -9.2098 & --- \\ 9.2098 & --- & --- & --- & 9.2098 & 9.2098 \\ --- & --- & -9.2098 & 9.2098 & -- & -9.2098 \end{bmatrix}$$

Step 4: Bit Node Processing

$L = [\text{Intrinsic Information} + \text{Extrinsic Information}]$

$$L_i = R_i + E_{j,i} \quad \text{-----} \quad (3)$$



This is the last step of decoding process. In order to get the final corrected codeword, one has to add probabilities of Intrinsic Information and Extrinsic Information.

Calculation of L Matrix is as shown in Table III.

TABLE III.CALCULATION OF L MATRIX

	Li	Ri+Ej,i	Values	Zi
I				
1	L ₁	R ₁ +E _{1,1} +E _{3,1}	-1.0986+9.2098+9.2098	17.321
2	L ₂	R ₂ +E _{1,2} +E _{2,2}	+1.0986-9.2098+9.2098	1.0986
3	L ₃	R ₃ +E _{2,3} +E _{4,3}	-1.0986-9.2098-9.2098	-19.518
4	L ₄	R ₄ +E _{1,4} +E _{4,4}	+1.0986-9.2098+9.2098	1.0986
5	L ₅	R ₅ +E _{2,5} +E _{3,5}	-1.0986-9.2098+9.2098	-1.0986
6	L ₆	R ₆ +E _{3,6} +E _{4,6}	-1.0986+9.2098-9.2098	-1.0986

$$Z = [L_1 \quad L_2 \quad L_3 \quad L_4 \quad L_5 \quad L_6]$$

$$Z = [17.321, 1.0986, -19.518, 1.0986, -1.0986, -1.0986]$$

$$Z = [0 \quad 0 \quad 1 \quad 0 \quad 1 \quad 1]$$

4. RESULTS AND ANALYSIS

This section presents Sum Product and Min Sum Algorithm based LDPC Decoder design results to demonstrate the effectiveness of the proposed decoder design. The coding of the Sum Product and Min Sum based LDPC Decoder design is done in MATLAB Version 14.1. The plot of Bit Error rate versus Eb/No is as shown in figure5 and 6. We demonstrate the performance of two algorithms with a block length of n = 724. The code rate is R = 1/2. The main objective of the paper is to increase the throughput of the decoder without degrading the error performance. With the use of Min Sum algorithm in partial-parallel configuration which accomplishes much savings in hardware utilization as compared to existing works.

Figure 5. Bit Error Rate Performance of the Algorithm for Code Lengths (1000, 500)

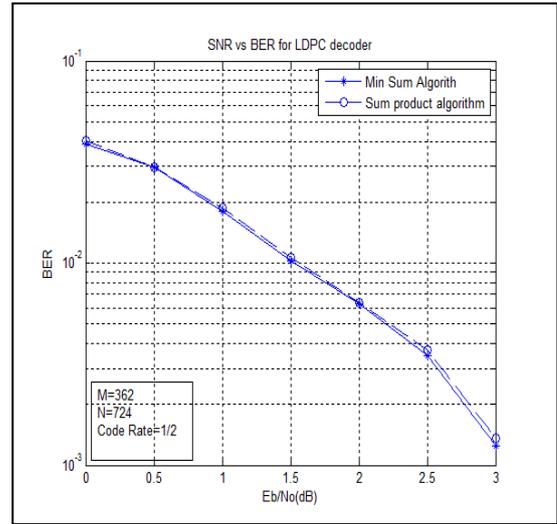


Figure 6. Bit Error Rate Performance of the Algorithm for Code Lengths (724,362)

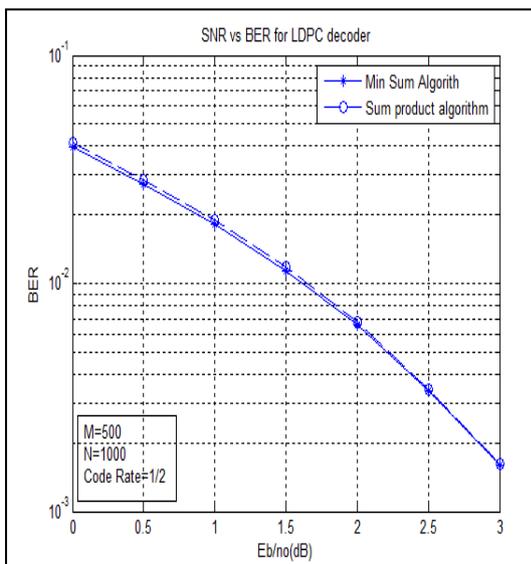


TABLE IV. FPGA DEVICE UTILIZATION SUMMARY

LDPC Decoder using Sum Product Algorithm				
Family:- SPARTAN 3 Target Device:- XC3S50				
SN	Designed Unit	Sum-product Algorithm		
	Features	Used	Available	Utilization
1	No. of Slices	42	768	5%
2	4 Input LUT's	77	1536	5%
3	No. of IOB's	29	124	23%

TABLE V.FPGA DEVICE UTILIZATION SUMMARY

LDPC Decoder using Min Sum Algorithm				
Family:- SPARTAN 3 Target Device:- XC3S50				
SN	Designed Algorithm	Min-Sum Algorithm		
	Features	Used	Available	Utilization
1	No. of Slices	28	768	3%
2	4 Input LUT's	52	1536	3%
3	No. of IOB's	21	124	16%



TABLE VI. COMPARISON OF SUM PRODUCT AND MIN SUM ALGORITHM BASED DECODER

LDPC Decoder			
Family:- SPARTAN 3			
Target Device:- XC3S50			
SN	Features	Sum Product	Min Sum
1	Number of Slices	42	28
2	4 Input LUT's	77	52
3	No. of IOB's	29	21
4	Throughput	1.46Gbps	1.14Gbps

TABLE VII. THROUGHPUT COMPARISON

Throughput Comparison			
Feature	[11]	[8]	This Work
Throughput	410 Mbps	522 Mbps	1.14Gbps

It also provides adequate level of bit error performance. Figure 5 shows the Bit Error Rate Plot versus Signal to Noise Ratio for the code length (1000, 500). The code rate is 1/2. Figure 6 shows the Bit Error Rate Plot versus Signal to Noise Ratio for the code length (724, 362). Table IV and V shows the FPGA Device Utilization statistics for LDPC Decoder using Sum Product and Min Sum Algorithm respectively. Table VI shows the Comparison of Sum Product and Min Sum Algorithm based Decoder and Table VII shows the comparison of throughput with existing works.

5. CONCLUSION

In this paper, we have presented detailed mathematical analysis of LDPC decoder and studied different types of message passing algorithms. The LDPC are coded in BPSK system and is implemented in HDL Verilog. The performance of Min-Sum Algorithm (MSA) is near to Sum-Product algorithm (SPA) and easy to implement in Verilog. The Verilog implementation of decoder was premeditated on SPARTAN 3 and device XC3S50. Throughput performance of Sum Product Algorithm based Decoder and Min-Sum Algorithm based Decoder is analyzed.

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