



# Circuit Techniques using Substrate Bias for Design of Radiation Hardened Voltage Controlled Oscillator

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**Abstract:** Radiation effect causes some major impact on CMOS devices, such as the switch point, change output rail voltage, and the increased leakage current. If radiation is high, proper inverter operation fails. We suggest a scheme to maintain the output voltage by making  $V_{gs}$  negative when the NMOS cuts off. This paper shows the structural CMOS with and without radiation and variation of electrical properties of device under various radiations doses and proposes a modified CMOS circuit which mitigates radiation effects by improving switch point in I-V characteristic. In order to redesign the circuit for radiation resistance; the above radiation hardened inverter circuit is implemented in each of Voltage Controlled Oscillator (VCO) gates using Radiation Hardened By Design (RDBD) technique.

**Keywords:** Radiation Hardened By Design (RHBD), Single Event Transients, Total Ionizing Dose, VCO, CMOS.

## 1. INTRODUCTION

There are a large number of photonic and particulate radiations existing in outer space. Depending on the energy of the particles, they affect semiconductor devices in a different way. X-Ray, Gamma Ray and heavy ions have enormous energy and generate electron-hole pairs in a semiconductor device [1]. The radiation effects on semiconductor devices are mainly classified as follows:

### A. Total Ionization Dose effects

Total Ionization Dose (TID) effects are a long term expose of radiation on active devices of electronic components. The total quantity of ionization dose depends on radiation intensity and amount. These effects cause some major impacts on semiconductor devices i.e threshold voltage variation due to holes trapped in  $\text{SiO}_2$  and  $\text{Si/SiO}_2$  surface change [2].

### B. Single Event Effects

Single Event Effects (SEEs) are due to single energetic particle strike the semiconductor device and may have in different forms. When this particle strike or transverse the device, transfers energy to the device material.

Single Event Upsets (SEUs) are soft errors, and non-destructive. It normally appears as transient pulse in logic circuits or bit error in memory flip flops or registers.

Several types of hard errors which are destructive can appear, Single Event Latch up (SEL) are hard errors and causes a high operating current than device maximum specified current and can only remove by power reset. Other hard errors may cause burnout of power MOSFETS, Gate Rupture, frozen bits, and noise in CCDs [1], [2].

Single event effects can be categorized into three effects (in order of permanency):

- a) Single Event Upset (soft error)
- b) Single Event Latch up (soft or hard error)
- c) Single Event Burnout (hard failure)

### C. Other Radiation Effects

In addition to threshold voltage variation and the single event effects, there are others radiation effects includes larger sub-threshold current, the larger leakage current and the degraded mobility. Digital circuits are mainly affected by this Single Event Effects and may upset the logic state of the circuit.

On the other hand the threshold voltage variation may appear in analog circuits and may affect the overall circuit performance [1]-[3].

Some major impacts on CMOS devices due to these radiation effects are the switch point deviation, the decreased output rail voltage, and the increased leakage current. If radiation becomes strong enough proper



inverter operation fails. We propose a scheme to maintain the output voltage by making  $V_{gs}$  negative when the NMOS cuts off [4].

This paper shows the structural CMOS with and without radiation, and variation of electrical properties of device under various radiations doses and proposes a modified CMOS circuit that mitigates radiation effect by improving switch point in I-V characteristic.

To redesign the circuit for radiation resistance; the radiation hardened inverter circuit is implemented in each stage of Voltage Controlled Oscillator (VCO) design [4], [5].

#### D. Simulation details

In Technology Computer Aided Design (TCAD) SEE mixed mode simulation, the incident particles must deposit enough energy to produce errors in the circuit output. The impact of incident particle induces the generation of hole-electron pairs. The recombination of the hole-electron pairs is generally modeled in SPICE by a double-exponential source current.

In case of particle strike, it is assumed that charge will be collected at susceptible node and a current generator is added in the circuit to model the charge collected on susceptible nodes. For ASICs, the sensitive nodes can be localized and the critical charge can be estimated from SPICE simulations.

The critical charge is the minimum charge collected to get an upset. Critical charge leads to evaluate threshold LET. Threshold LET is mainly used to characterize the SEU sensitivity of a circuit. It can be measured with a particle accelerator to give the cross section LET curves. The goal is to evaluate it by SPICE simulation. The relation between the critical charge and the threshold Linear Energy Transfer ( $LET_{th}$ )

$$Q_{crit} = \frac{q \cdot \rho}{E_{e,h}} L_f \cdot LET_{th} \quad (1)$$

With:

- $q$ : Electron charge ( $1.6 \times 10^{-19}$  C).
- $\rho$ : Material density ( $2.33 \text{ g/cm}^3$ ) for silicon.
- $E_{e,h}$ : Energy needed to create electron-hole pairs ( $3.6 \text{ eV}$ ) in silicon.
- $L_f$ : Funnel length (m).

Ionizing effects like SEU is strongly associated with the transient analysis statement .TRAN. For this reason, the .RAD statement must be coupled at least with one .TRAN statement. Set directly the maximum Current  $I_{SEU}$  of Messenger's equation and computes the maximum current using the equation of deposited charge defined above.

In this circuit, the LET value of the incoming strike is set up as a variable, by the line "set LET=1", which

creates a variable called "\$LET" and assigns it a unity value. A second variable called "\$density" is assigned.

Lastly, the key syntax in any SEU simulation is the singleeventupset statement, which is used to specify entry and exit points, radius and density of the electron-hole pair distribution generated by the particle track.

In this simulation, a C-interpreter function is used to define photo-generation rate in text file that can be attached to the program. The time and position dependable photo generation rate define in file and return to program. This return value is multiplied at each node point.

The coordinates of the starting and the last point of the line segment set the parameter, The X. ORIGIN, Y. ORIGIN and X. END, Y. END. For the top left and bottom left corners of the device, the defaults value is considered.

The Standard beam input syntax allows specification of plane waves with Gaussian or flat-top (top-hat) irradiance profiles.

It is assumed that the radiation on the CMOS latch up device has created a uniform photo-generation rate of  $1 \times 10^{25} \text{ s}^{-1} \text{ cm}^{-3}$  within the CMOS device.

The circuit design and simulation of VCO has done using analog and mixed signal simulation tool.

## 2. CMOS STRUCTURES AND CHARACTERISTICS WITH AND WITHOUT RADIATION

### A. Device Level Simulation

In unhardened devices, the latch up problem appears in CMOS bulk devices (ICs) due to parasitic four-layer PNP path. Once latch appear then there is only way to turn off the latch up by shutting off the power

If PNP structure or parasitic SCR appears in CMOS bulk device and this excessive charge may cause a latch up and direct to SEL which may lead to destruction of the device.

Another important catastrophic SEE event called "snapback" shows many of the characteristic of latch up and may appear in single MOS transistor structure.

A single high energy particle may causes snapback if the field across the drain region is sufficiently high.

The transversal of the heavy ion cosmic ray particle caused a parasitic bipolar transistor existing between the drain and source region of a MOS transistor which amplifies avalanche current and a very high current between the drain and source region of the transistor is generated with subsequent localizing heating.

The uniform photo-generation rate of  $1 \times 10^{25} \text{ s}^{-1} \text{ cm}^{-3}$  is defined using C-INTERPETER function as shown on the Figure 1.

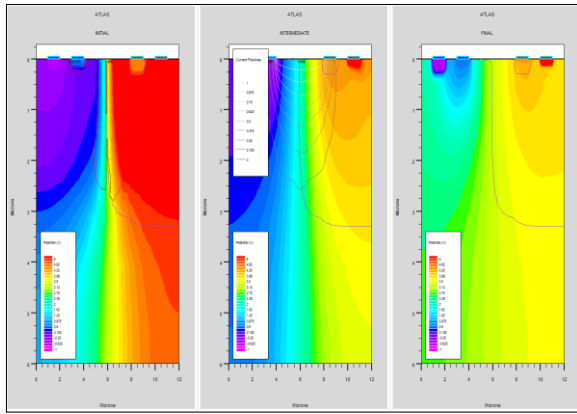


Figure 1. Initial, Intermediate & Final Potential Contour Plots of CMOS Device with Radiation.

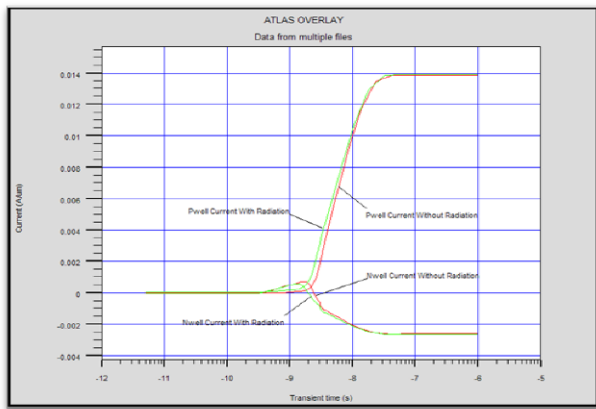


Figure 2. Transient P well & N well current Simulation of CMOS Device with and without Radiation.

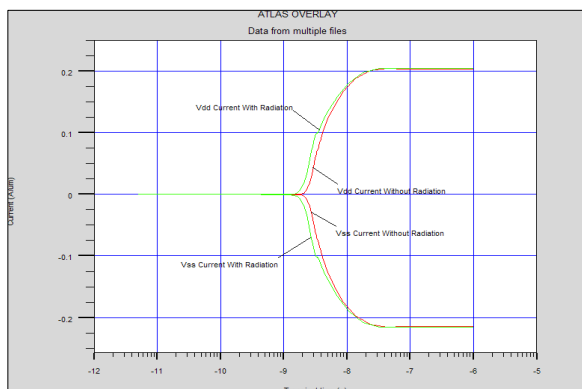


Figure 3. Transient  $V_{dd}$  &  $V_{ss}$  current Simulation of CMOS Device with and without Radiation.

### B. Circuit Level Simulation

As shown in figure 4, the inverter circuit uses the mixed mode module to simulate the circuit performance of inverter using SPICE level 1 models.

There are four separate runs in the input file. In the first, the construction of an NMOS transistor syntax uses the mesh, region, and electrode coordinates in the syntax are specified. i.e. When the structure is defined in mixed mode, it is mandatory to define the electrode name. Several Gaussian and uniform analytical functions are defined for the doping distribution in device construction. The final structure is saved for later use.

In the second run, the initial operating point of the circuit is calculated and the syntax is divided into two parts. The first part is a SPICE-like circuit description and control cards. The second is the device parameter syntax. The circuit netlist is written using standard SPICE syntax.

A single DC operating point is solved in the second run to make an initial guess for the third run. In the third run, the command `.dc` is used to set a DC ramp of the input voltage ' $V_{in}$ ' from zero to 5.0V in 0.25V steps at each node. Current and voltage are saved in the file specified in the `.log` statement.

In the final run, the `.tran` statement combined with a time-dependent definition of ' $V_{in}$ ' using the PULSE parameter to set up a switching transient are used. The pulse of ' $V_{in}$ ' has a peak value of 5.0V, a rise and fall time of 50ps, and a time at peak value of 1ns are specified in the PULSE syntax and 1ps specifies the initial time step only are specified on the `.tran` statement. All other time steps are automatically calculated by Atlas and it differs from the `.tran` card in standalone SPICE programs. The maximum simulation time is set to 3ns.

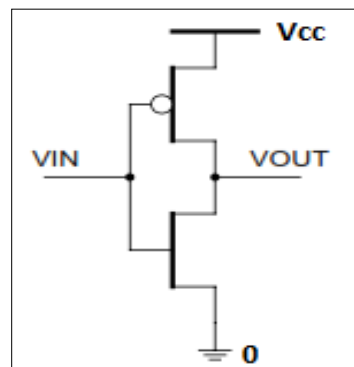


Figure 4. Inverter Circuit

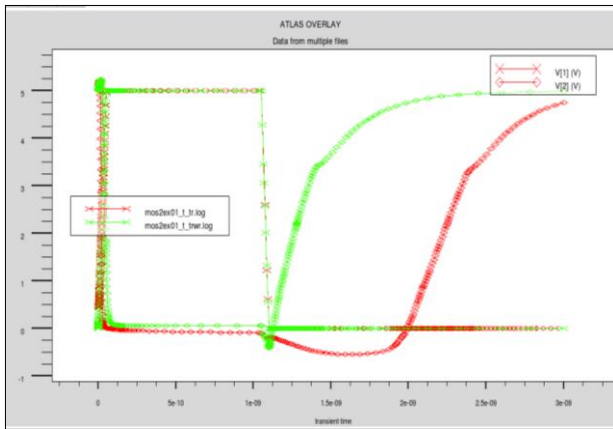


Figure 5. Input v/s output curve under radiation

As shown in the basic CMOS inverter circuit under stimuli of different radiation doses, the switch point deviation, the decreased output rail voltage and the increased leakage current variation are the most important changes because of threshold voltage variation. If radiations are strong enough than device switching operation may fail.

C. Rad-Hard Inverter Circuit

In design of Rad-hard inverter circuit which is modified to basic inverter circuit shown in figure 4. Mixed mode module is used to simulate the circuit performance of two NMOS inverters as shown in circuit in figure 6. The first inverter is simulated using Atlas, the second inverter using SPICE level 1 models

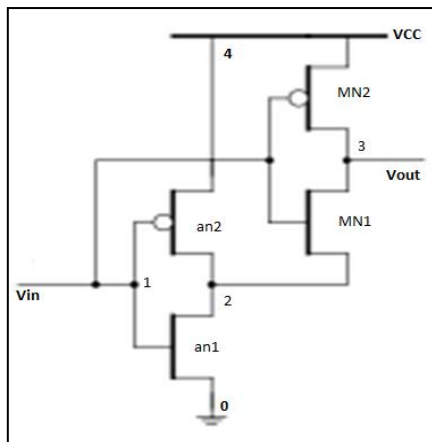


Figure 6. Rad-hard Inverter circuit

In mixed mode simulation, transistors are define in different way, the first NMOS transistor labelled “an” and syntax specified the structure file name from the previous run for this transistor. Connect circuits node to structure node specified in previous run. The other

NMOS transistor labelled 'mn' is simulated using SPICE level 1 model and sets the models, material and contact parameters for the device.

The second run solves a single DC operating point as the initial guess to the third run. The third run uses the command .dc to set a DC ramp of the input voltage 'Vin' from zero to 5.0V in 0.25V steps. The currents and voltages for each node are stored in the file specified in the .log statement.

The final run uses the .tran statement combined with a time dependent definition of 'Vin' using the PULSE parameter to set up a switching transient. The PULSE syntax specifies that the pulse of 'Vin' has a peak value of 5.0V, a rise and fall time of 50ps, and a time at peak value of 1ns. On the .tran statement, 1ps specifies the initial time step only. All other time steps are automatically calculated by Atlas. This differs from the .tran card in standalone SPICE programs. The maximum simulation time is set to 3ns.

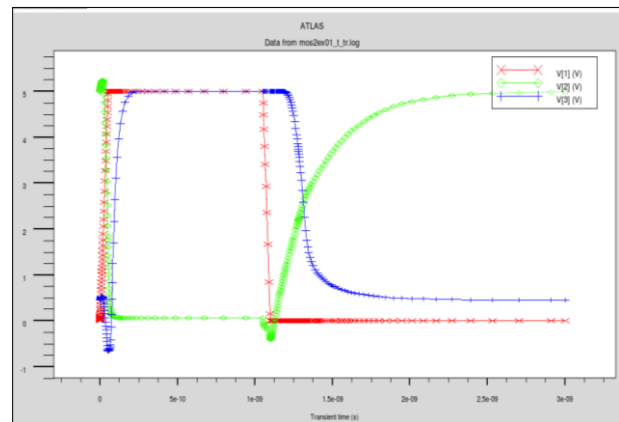


Figure 7. Simulation of Rad-Hard Inverter Circuit with Radiation Effects

Modified inverter circuit irradiated and found that the additional PMOS and NMOS transistor keep the original NMOS cut off when the input is low and maintain the proper operation when input is high.

3. DESIGN OF RADIATION HARDEN VOLTAGE CONTROL OSCILLATOR (VCO) USING CMOS PROCESS

One of the most important design specifications for a VCO is its frequency versus control voltage characteristic. If this characteristic changes due to radiation, it can affect the central frequency of the VCO as well as its tuning range resulting in an unstable PLL, where VCO used. Therefore in the presence of radiation, it is desirable to have a VCO of which the frequency remains unchanged at a given a control voltage. Keep in mind of above problem; we switched over to Radiation Hardened Circuit [6]-[8].

The VCO circuit shown in figure 8 has two current controlled ring oscillators M12-M23 and M24-M35 used for noise rejection.

In every ring oscillator to make rad hard, design includes three inverters and each inverter consists of four transistors. The total current of oscillators is provided by M3 and M5-M8 and transistor M3 converts the control voltage to current while M5-M8 provides minimum current for ring oscillators when M3 is off. The sum of the current is mirrored through M10, M11 and then controls the ring oscillators. The cross coupled transistors M28, M29 synchronize the two oscillators so that the outputs are 180° degrees out of phase which are required. The simple diff-amp (M38-M42) converts the outputs of two ring oscillators to a single ended value and restores the VCO output voltage swing to full rail-to-rail output[4],[8].

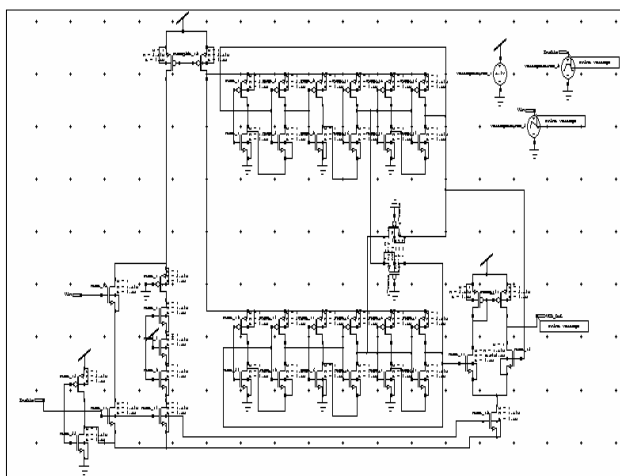


Figure 8. Radiation Hardened VCO circuit.

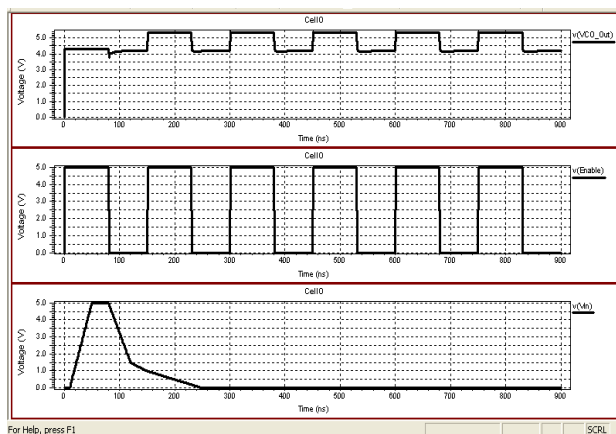


Figure 9. VCO Output

## CONCLUSION

This paper focuses on the simulated results for the radiation hardened CMOS inverter. The first section shows the simulation results prior to radiation and post radiation using radiation hard model file and second section shows the radiation harden by Design (RHBD) Voltage Control Oscillator (VCO) circuit simulation. It is shown that TID and SEE effect changed the threshold voltage of both NMOS and PMOS transistors by about 0.2 V. Post radiation simulation shows the basic degradations of inverter performance due to radiation effect. Accordingly, this simulation can help optimize our radiation hard circuit design of VCO.

## REFERENCES

- [1] Maximilien Glorieux, Adrian Evans, Veronique Ferlet-Cavrois, Cesar Boatella-Polo, Dan Alexandrescu, Sylvain Clerc, Gilles Gasiot, and Philippe Roche, "Detailed SET Measurement and Characterization of a 65nm Bulk Technology", IEEE Transactions on Nuclear Science, Volume: PP, Issue: 99, December, 2016
- [2] Matthew J. Gadlage, Jonathan R. Ahlbin, Peter Gadfort, Austin H. Roach, and Scott Stansberr, "Characterization of Single Event Transients in Schmitt Trigger Inverter Chains Operating at Sub-threshold Voltages", IEEE Transactions on Nuclear Science, Volume: PP, Issue: 99, December 2016
- [3] Jeffrey Prinzie, Jorgen Christiansen, Paulo Moreira, Michiel Steyaert, Paul Leroux, "Comparison of a 65 nm CMOS Ring- and LC-oscillator Based PLL in terms of TID and SEU sensitivity", IEEE Transactions on Nuclear Science, Volume: PP, Issue: 99, December 2016
- [4] Sanchez Esqueda, H. J. Barnaby, M. P. King, "Compact Modeling of Total Ionizing Dose and Aging Effects in MOS Technologies", IEEE Transactions on Nuclear Science, Volume: 62, Issue: 4, Aug. 2015.
- [5] L. Artola, G. Hubert, M. Raine, P. Paillet, "Modeling Single Event Transients in Advanced Devices and ICs", IEEE Transactions on Nuclear Science, Volume: 62, Issue: 4, Aug. 2015.
- [6] R. C. Laco, "The effects of total ionizing dose irradiation on CMOS technology and the use of design techniques to mitigate total dose effects", in Proc. Reliability Physics Symp., 2002, p. 376.
- [7] Dong Pan, Harry. W. L. Bogdan. M. Wilamowski, "A Radiation-hard Phase-Locked Loop", IEEE 2003.
- [8] Jer-Fu Dennis Wu, "Phase locked loop for radiation hardened Environment", The University of Texas at Arlington, Dec. 2006

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C. P. Jain obtained B.E, M.Tech and PhD in Electronics Engineering. Worked with Public Sector Company for 2 years and presently involved in teaching and research for last 15 years. Areas of interests are Devices and Circuits under extreme environment applications.