Multi-Level Inverter Based UPQC for PQ Enhancement of Distribution System Under Contingencies

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Abstract: Distribution systems are prone to faults, voltage unbalance, and harmonics since there is a tussle of loads, particularly power electronic based. Unified Power Quality Conditioner (UPQC) is a versatile power conditioner dedicated to distribution systems since it can mitigate almost all types of PQ issues. Conventional-UPQC (C-UPQC) is designed with three-phase VSC. However, it is unable to mitigate the unbalance in the system completely, and the distortion in voltage and current waveforms still exists. To address the above issues, in this paper, UPQC is designed using a Multilevel Inverter (MLI) with a Neutral Point Clamped (NPC) based converter topology generating 5-level inverter output. In this paper, modified NPC topology is presented in which the capacitor connected across all three phases of the inverter is reduced, and a balance in capacitor voltage is obtained by employing the SPWM carrier-based modulation technique. The proposed NPC-MLI-UPQC is designed using the right shunted topology to protect the source profile from harmonics injection via non-linear loads. The control of MLI is so designed to obtain the harmonic-free output. The performance of the proposed NPC-MLI-UPQC has been analyzed for linear non-linear for the various contingencies generated due to fault conditions resulting in sag as well as swell in voltage.

Keywords: Custom Power Devices (CPD), Multi-Level Inverter (MLI), Neutral Point Converter (NPC), Power Quality (PQ), Power Electronic Converter (PEC), Unified Power Quality Conditioners.

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1. Introduction

The modern power system is the era of technological advancement, leading to the high penetration of Power Electronics (PE) into the Conventional Utility System (CUS) [1, 2]. The PE has both positive and negative effects on CUS. The increased application PE is due to PE interfaced renewable generation, PE based Controllers to control power flow within the CUS, FACTS controllers, and a new concept of "Flexible, Reliable and Intelligent Electric Energy Delivery System" (FRIENDS) discussed in [4] which supports the desirable structure to incorporate distributed generation within the CUS. All these aspects present the proliferation of PE in CUS, particularly at distribution side because at distribution level only high penetration of PE is witnessed in the form of non-linear loads or distributed generation [3]. The high PE penetration can adversely affect the system stability. It results in reduced transient stability limits since conventional synchronous generation based generation is being replaced by unconventional generations like solar or wind which does not have inertia limits. When properly controlled PE can also present a feasible solution for stability issues generated due to its high penetration. This paper presents one such smart power conditioning device designed via PE which has been widely adopted in distributed system. The Unified Power Quality Conditioner (UPQC) is a Customized Power Device (CPD) which can regulate the power quality issues such as unbalanced supply voltage, harmonics, voltage sag/swell, unbalanced loading, etc. [5-7].

Hingorani [8] has introduced the concept of CPD for enhancing Power Quality (PQ) in distribution system. CPD are application oriented and their zone of influence is small, limited to the reach of their operation. Therefore; CPD are specifically customized for the distribution system. UPQC is one of the widely adopted CPD in distribution system which have dual compensating scheme actualizing the following control plot [9]: 1) it's shunt converter is controlled for voltage mode in order to maintain terminal voltage at all operating condition; 2) series converter is controlled for current mode to maintain sinusoidal line current, and 3) control of series-shunt converters as an extensive impedance control mode (subsequently constraining the line current amid utility voltage limits). Seeing to its wide area applications, a lot of researchers have worked in designing and controlling UPQC since it can be easily configured as per the requirement [10-15]. If active power is to be controlled, UPQC-P topology is designed, reactive power and complex power are dedicatedly controlled through UPQC-Q and UPQC-S respectively. For the source voltage sag/swell mitigation UPQC-R is used in which right converter is shunted and for protecting sensitive and critical loads from voltage unbalances and fluctuation at the source side UPQC-L is used where left side converter is shunt [16].

Conventionally UPQC is designed using 2-level (2-L) Voltage Source Converters (VSC) if operated in voltage control mode, or Current Source Converter (CSC) when operated in current control mode. The 2-L VSC/CSC has low voltage range application and cannot be used for precise control with high sensitivity. In this work, converters of UPQC are designed using MLI [17]. MLI has improved harmonic characteristics and the high level of precision with zero magnetic interference even at high switching frequencies. MLIs are broadly of three types; Flying Capacitor (FC), Neutral Point-Clamped (NPC) and H-bridge cascaded type (CHB) topology [18]. Among these, the component requirement of FC is high which limits it's application and CHB has better performance characteristics, but it requires individual source across each H-bridge unit which increase the source requirement and control becomes complex. Hence NPC is very compatible in terms of performance efficiency and component requirement [19].

In this paper 5L NPC-MLI converter is designed for the UPQC-R controller. The UPQC structure comprises of the two converters, one connected in series suppling rectified sinusoidal current. The other one is in parallel supplying rectified sinusoidal voltage source. Series converter must have high impedance to block the harmonic currents generated by nonlinear loads. On the other hand parallel converter must have low impedance to absorb the load harmonic currents.

The proposed UPQC-R topology can perform the following functions;

- Simultaneous voltage and current harmonic mitigation under various dynamic conditions of voltage sags, non-linear load, unbalanced load, etc.
- Improved load current compensation due to use of MLI topology and d-q control of UPQC-R.
- Continuity of supply and stable operation in the condition of voltage interruption.

The proposed NPC-MLI-UPQC has been simulated in MATLAB-Simulink software and operated under various abnormal conditions of non-linear loading and symmetrical and unsymmetrical system faults. A comparative analysis is also presented of the proposed topology with the conventional 2-L UPQC. The controller of NPC-UPQC is designed with sinusoidal synchronous reference frame (SRF) theory, in which grid voltage is considered as the reference signal to generate the gate pulses for the PE switches. The detailed controller architecture is presented in section 4 for NPC-MLI whereas for conventional 2L-UPQC controller architecture is discussed in section 2 with simulation results presented in section 3 for 2L-UPQC and in section 4 for 5L-NPC-MLI-UPQC results are presented. Section five discusses the results in details and section six concludes the research findings of the paper.

2. Unified Power Quality Conditioner (UPQC)

UPQC is a two-converter device which is connected between source and load and designed dedicatedly for ESS. It provides simultaneous series shunt compensation and gaining popularity as a compensating device to obtain high PQ output which meets all the standards and specifications at the POI as per the grid code requirement [20]. UPQC combines series as well shunt converter wherein isolation-transformer connects the series converter between source and load and behaves as an ideal VSC injecting series voltage. While shunt converter is directly shunted across the load and behaves as an ideal current-source converter which injects shunt current. The detailed circuit topology of the UPQC is given in Figure 1. Series converter eliminates the load current harmonic using series inductor of filter element, the series-shunt combination of converters makes sure of no real power injection and absorption from UPQC and it only means for reactive power compensation [20].

Most of the topologies reported in the literature are developed by using a conventional 2-L VSC/CSC [21], which limits its application to low voltage level. But the mitigation of PQ problems in medium voltage at the distribution side is also essential, due to the increased use of industrial, non-linear load and distributed generation. To improve the performance of the UPQC this research presents the MLI based converter topology.

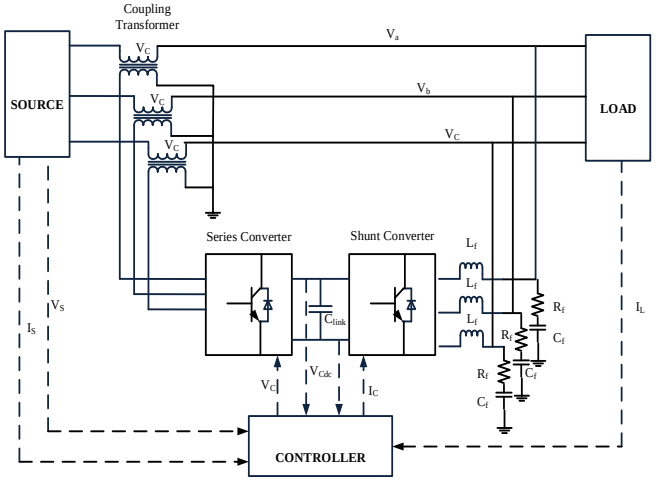

Figure 1. Detailed circuit topology of UPQC.

2.1. Control of Series Converter

Series converter maintains the sinusoidal source current waveform by blocking the injection of harmonics from load side by providing high impedance path. It also compensates source voltage disturbances which may be the result of line faults. The source voltages as reference are fed and detected by the control which is then transformed to dq0 equivalent 3Φvalues using Eq. (1) [15];

$$[V_{dq0}] = X[V_{abc}] \tag{1}$$

Where;

$$X = \sqrt{\frac{2}{3}} \begin{bmatrix} cos\theta & cos(\theta - 120°) & cos(\theta + 120°) \\ -Sin\theta & -sin(\theta - 120°) & -sin(\theta + 120°) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \tag{2}$$

The main task of series converter is to keep load bus voltage constant to its peak value irrespective of the source condition, that means;

$$V_{Ldq0} = \begin{bmatrix} Vm \\ 0 \\ 0 \end{bmatrix} \tag{3}$$

Where; V_{Ldq0} is load bus voltage in dq0 frame and Vm is peak voltage of the system. This means that only direct-axis load voltage exists and other two remains zero. The reference voltage after compensation is presented in Eq. (4) as obtained from the general control architect of the series converter as presented in Figure 2.

$$V_{dq0} = V_{Ldq0} - V_{Sdq0} \tag{4}$$

The compensated reference voltage is then transformed into its equivalent three-phase by using Inverse Park's transform. The output is synchronized using PLL which calculates the phase angle θ.

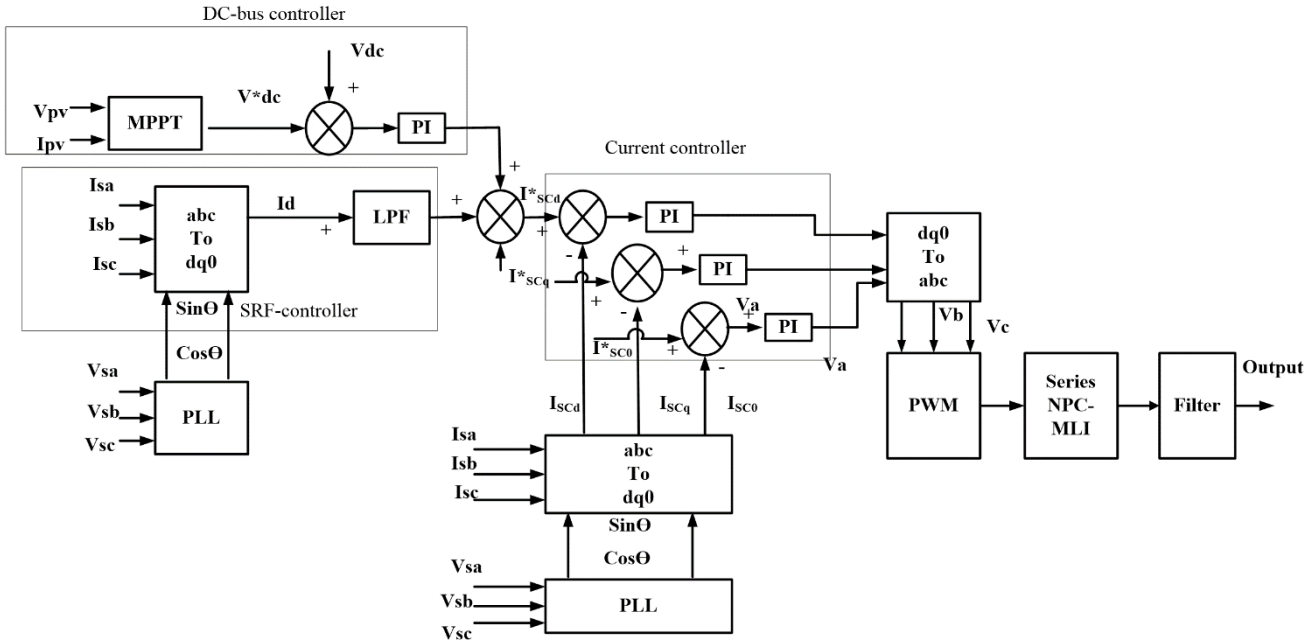

Figure 2. Control of series converter.

2.2. Control of Shunt Converter

Use Shunt converter compensate load-current harmonics which may be due to non-linear load or other abnormal and inject active-power into the system even if supply interrupts at source side [22]. The sensed 3-Φ load current is then transformed from abc to dq0 equivalent values using Eq. (5). It converts the fundamental positive-sequence component into equivalent DC, which can further be extracted using LPF and all the harmonics are filtered to ground. Hence load current can be obtained by Eq. (6).

$$[I_{dq0}] = X[I_{abc}] \tag{5}$$

$$I_L = I_c + I_s \tag{6}$$

Where; I_c is converter current and I_s is the source current supplied by utility system to the UPQC. PI controller maintains the fluctuation in DC-bus voltage, which is given input as error quantity between the desired value of capacitor and actual value. A small DC value ΔI_{dc} is added to the current in order to obtain new d-axis reference value as shown in Eq. (7).

$$I_{dc\_ref} = I_{dc} + \Delta I_{dc} \tag{7}$$

Where; ΔI_{dc} is the error value, I_{dc_ref} is the reference DC-current and I_{dc} is the fluctuated DC current in DC-link. The control architecture of shunt converter is presented in Figure 3.

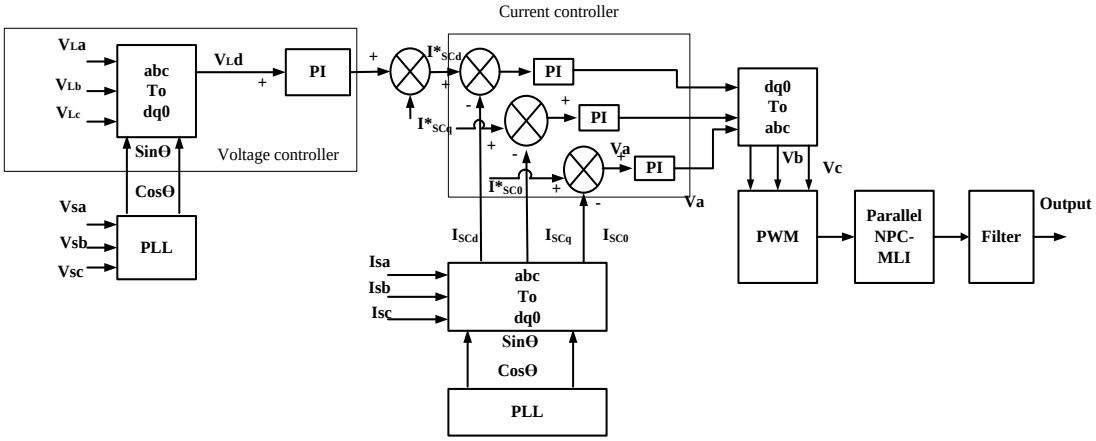

Figure 3. Control of shunt converter.

4. Performance Analysis of conventional 2L-UPQC

Generally, UPQC has two-modes of operation; one is normal mode, in which case the voltage supplied by UPQC is same as the voltage demanded i.e.

$$V_L = V_m = V_S \tag{8}$$

In this case injected voltage requirement from the converter is nil. While drawing phasor for UPQC in this mode, suffix 1 is added to current and voltage quantities as shown in Figure 4. From the phasor-diagram it can be observed that the load always draws the in-phase positive sequence component from the source through series converter. For non-linear loads, shunt converter supplies the required compensation in this mode.

Another is compensating mode; In this mode, the compensation is provided by the UPQC for the mitigation of voltage disturbances. UPQC injects the required voltage V_{inj} to the load for maintaining V_m. While drawing phasor for UPQC in this mode, suffix 1 is added to current and voltage quantities as shown in Figure 5.

For a constant demand of active power;

$$V_{S1}I_{S1} = V_{S2}I_{S2} \tag{9}$$

Hence shunt converter compensation current could be;

$$I_{S2} = \frac{V_{S1}I_{S1}}{V_{S2}} \tag{10}$$

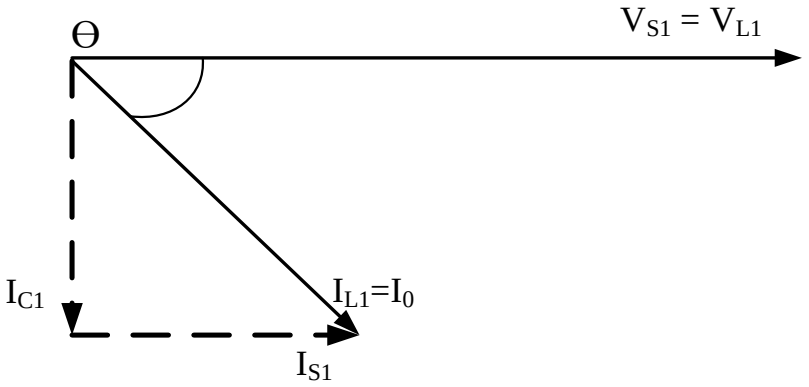

Figure 4. Phasor diagram of UPQC under normal operation.

Where;

V_L = Load voltage
V_m = Peak voltage of system
V_S = Source voltage
I_{S1} = Source current
I_{C1} = Current injected by converter
I_0 = Output current at PCC
Θ = Phase angle between load voltage and current

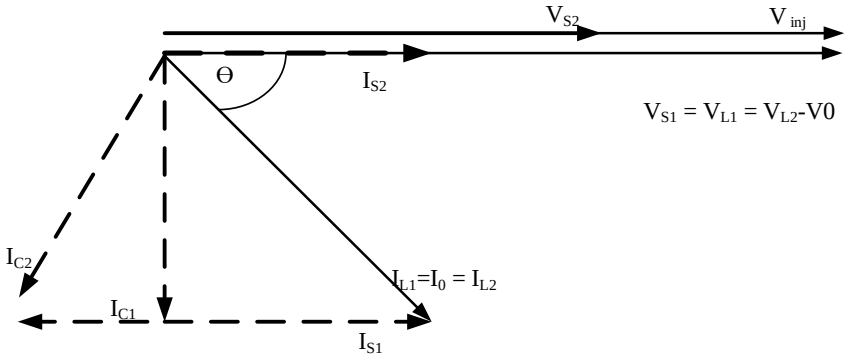

Figure 5. Phasor diagram of UPQC under the condition of voltage disturbances.

This section presents the performance analysis of conventional 2L-UPQC under both the normal mode and the compensating mode. The conventional 2L topology of UPQC is designed for current control mode and is connected to the 11kV 3-Φ distribution system. The performance of the system is analyzed in MATLAB Simulink toolkit. The system has been designed for 11 kV RMS for a peak value of 15.5 kV. The design parameters for 2L-UPQC system are presented in Table 1.

Table 1. Design parameters for 2L-UPQC and 5L-NPC-MLI-UPQC.

Parameter	**2L-UPQC**	**Proposed NPC-MLI-UPQC**
RMS Utility voltage V_{PH}	11 kV	11 kV
Peak Utility voltage V_{PH}	15.5 kV	15.5 kV
Grid frequency f_S	50Hz	50 Hz
Switching frequency of the converters f_{ch}	2.5 kHz	2.5 kHz
DC-link Coupling capacitance	9600 µF	9 µF
DC-link voltage balancing capacitance and unit per converter	--	1 mF and 3 units per converters for all the three phases
Filter Inductances	16 mH	16 mH
Filter Capacitances	450 µF	300 µF
Filter resistances	0.1 Ω	0.1 Ω
Inductance of the series coupling Transformer	1000 mH	1000 mH
Resistances of the series coupling transformers	21 Ω	21 Ω
dc-bus voltage Vdc	7500V	5000V
PI gains	Kp = 0.04; Ki = 500	Kp = 0.04; Ki = 500

UPQC is connected between source and load, hence source side, as well as load side voltage and current will be analysed under various contingencies conditions for linear as well as non-linear loads. A linear load of 150 KW with 1000 inductive reactance is connected at load bus. Under the condition of linear load system retains its normal operation with source as well as load voltage and current as shown in Figure 6 and Figure 7 respectively. The system is operating at normal condition hence, UPQC operates under normal mode feeding the load the required active and reactive power. The active power flow is 150 KW and graph has some initial transients which settles upto 0.1 sec as shown in figure 9. The reactive power at load bus is approx. 90 kVA which accounts the load power as well as reactive power required by the system including transformer and converters of the UPQC. The grid voltage THD is 0.01 % and load voltage THD is 1.0 % as shown in Figure 8. The voltage THD is within specified limits of Central Electricity Authority (CEA). The power factor in this case is 0.97 PU.

Now, the system has been analysed for non-linear loads with contingencies. UPQC has the capability to compensate voltage disturbance whether in the form of sag/swell/interruption or flickers. By employing UPQC constant voltage can be obtained using series converter functioning as DVR, even though the other side of the bus has high voltage fluctuations. Also, it can be simultaneously employed as STATCOM mitigating voltage and current harmonics both in voltage and current profile. To analyse the performance of the UPQC, a condition of voltage sag is created at source side using three phase to ground fault for the duration of 0.26-3 sec. Also, frequent fluctuations are created in the source voltage resulting in simultaneous voltage sag and swell as shown in figure 11. For 0.03-0.06 sec source voltage undergoes dip, for 0.1-0.16 sec condition of voltage swell is generated upto 1.5 times of the rated value, for 0.2-0.25 sec source undergoes interruption. Simultaneous variations can be seen in source current as shown in figure 12. The THD graph for the contingency source and non-linear loading condition is shown in figure 13. The THD graph of source voltage is obtained at the point when voltage swell occurs hence the magnitude of voltage in THD graph is 1.5 times of 1.55, which is 2.3 kV and THD percentage is 9.3 %. At this point, THD of grid current is 3.45% and power factor at load bus is 0.94 PU. UPQC mitigates the source voltage fluctuations and keeps the load voltage at the constant rated value as shown in figure 14. At load bus three phase rectifier is connected which generates highly distorted load currents whose THD is very high of the order of 29 % as shown in figure 15.

The abnormal operating condition of non-linear loading and various system faults, adversely effects the performance of CUS leading to the generation of various PQ issues. Though proposed 2L-UPQC is capable of regulating load voltage when source is undergoing frequent fluctuations and also, the harmonics in source currents are been blocked by shunt converter of UPQC-L. But, the reactive power demand of the converters are too high of the order of 3MVA. Hence a modified NPC topology for 5L MLI is developed in this paper for designing MLI-UPQC which has been discussed in next section.

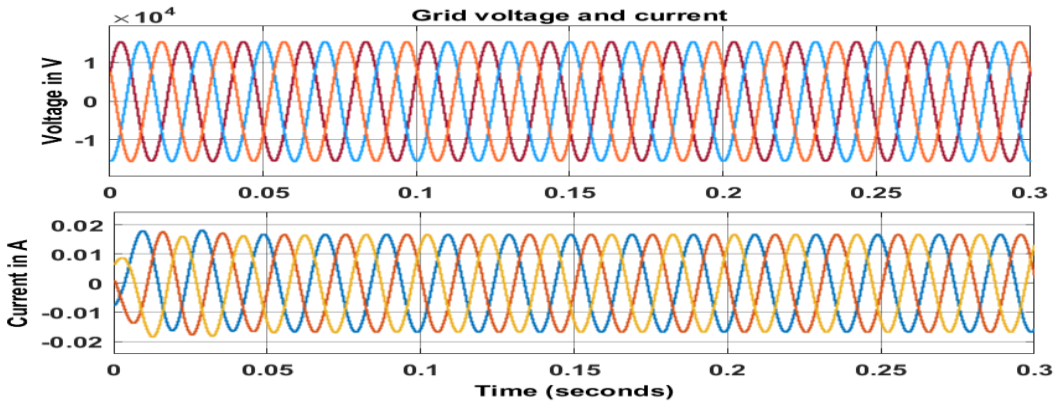

Figure 6. Source bus profile for linear load under normal mode of 2L-UPQC.

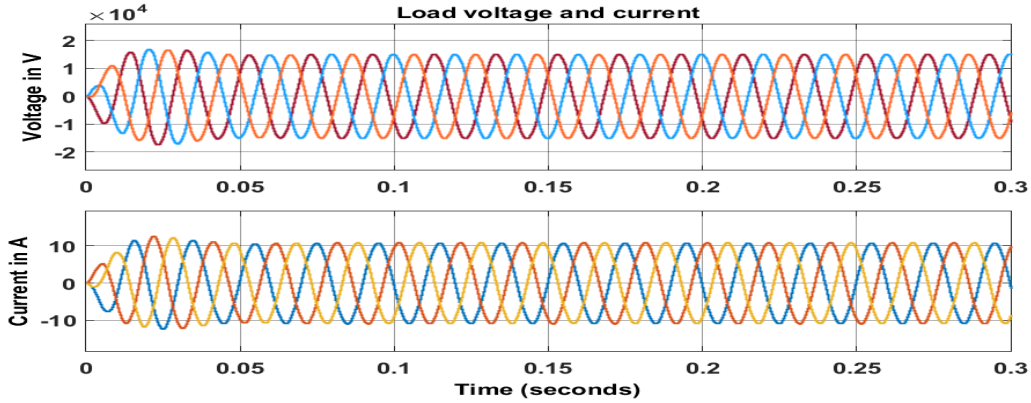

Figure 7. Load bus profile for linear load under normal mode of 2L-UPQC.

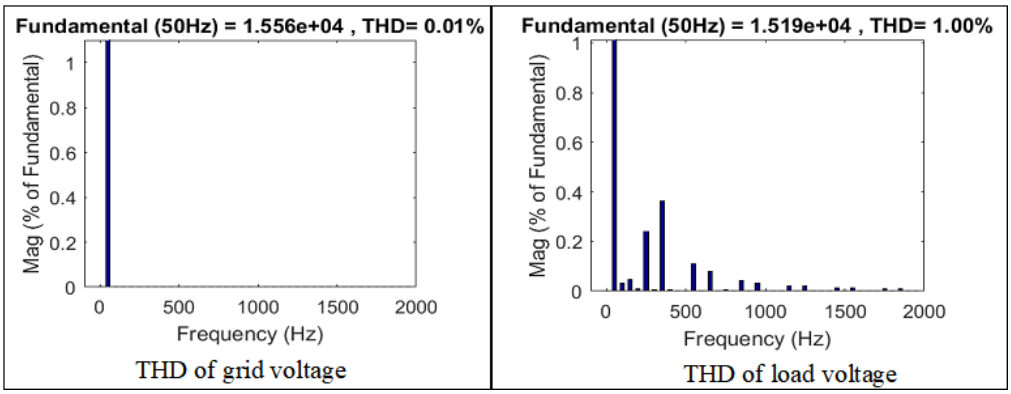

Figure 8 THD of grid voltage and load voltage for linear load.

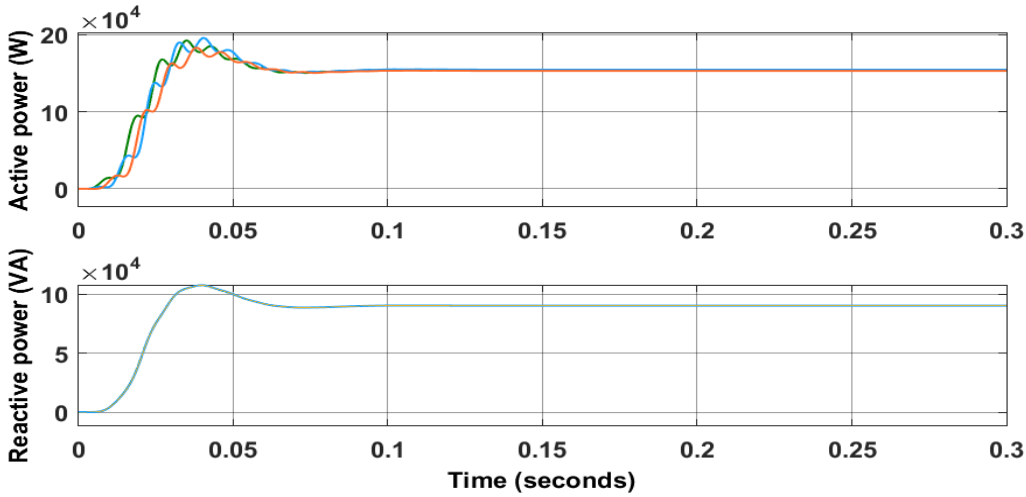

Figure 9. Active and reactive power for linear load under normal mode of 2L-UPQC.

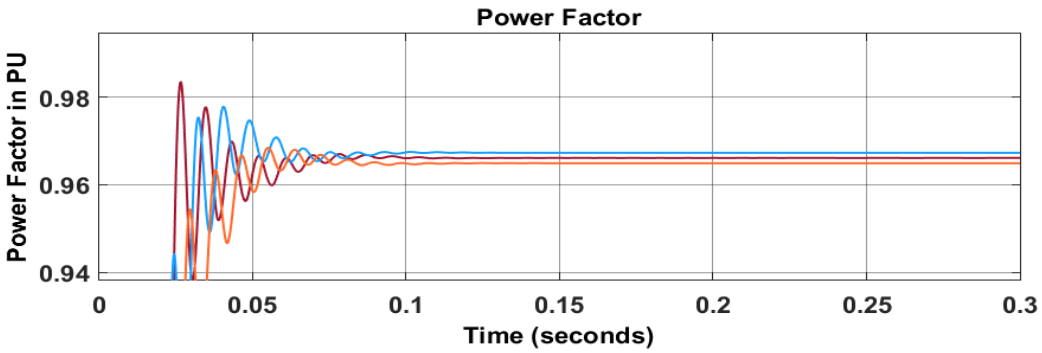

Figure 10. Power factor for linear load at load bus.

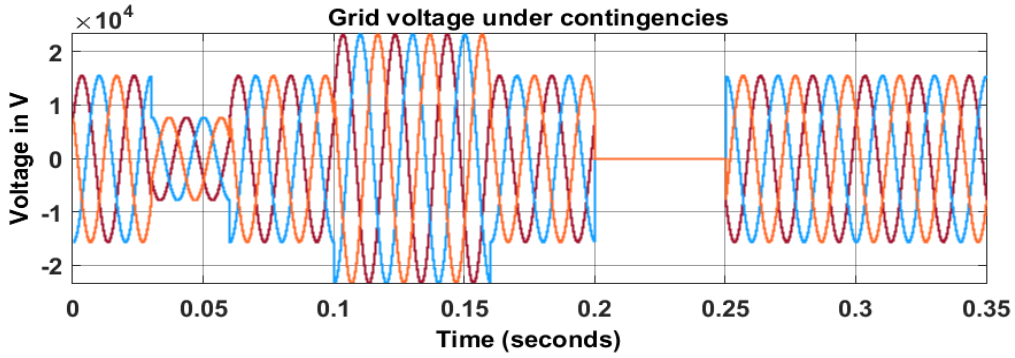

Figure 11. Source voltage profile for non-linear load under the contingencies.

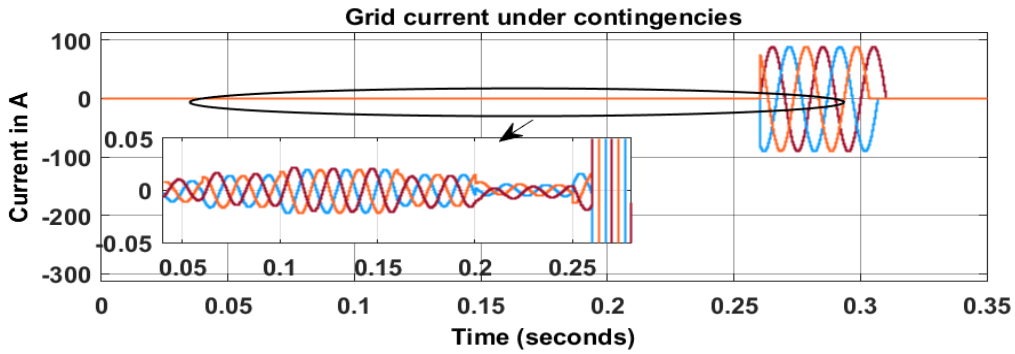

Figure 12. Source current profile for non-linear load under the contingencies.

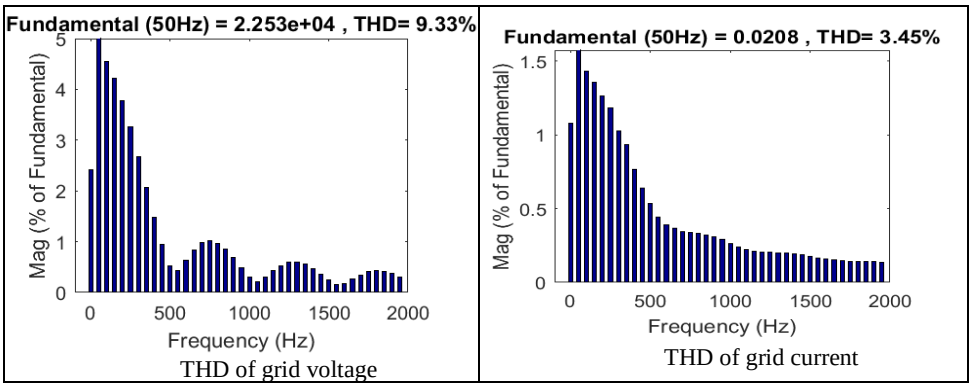

Figure 13 THD of grid voltage and grid current for non-linear load and source side contingencies.

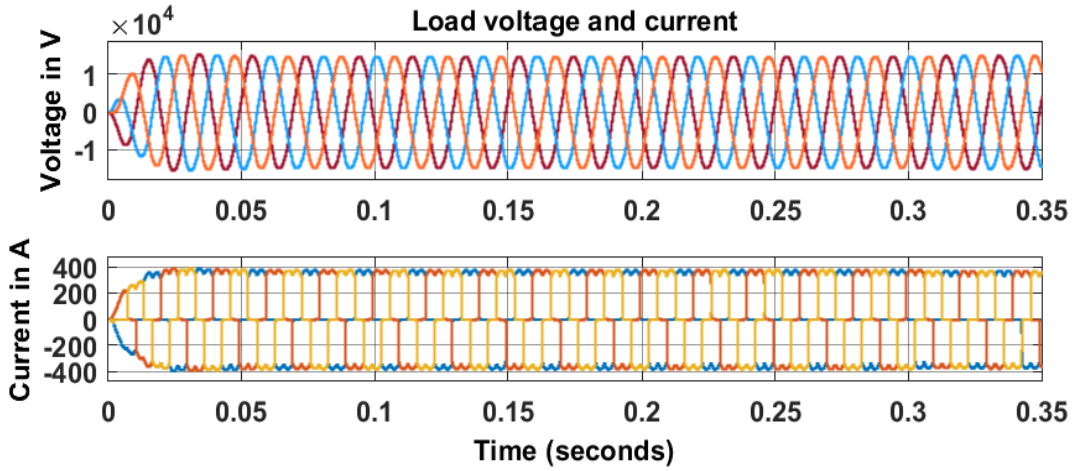

Figure 14 Load profile for non-linear load under the contingencies with 2L-UPQC.

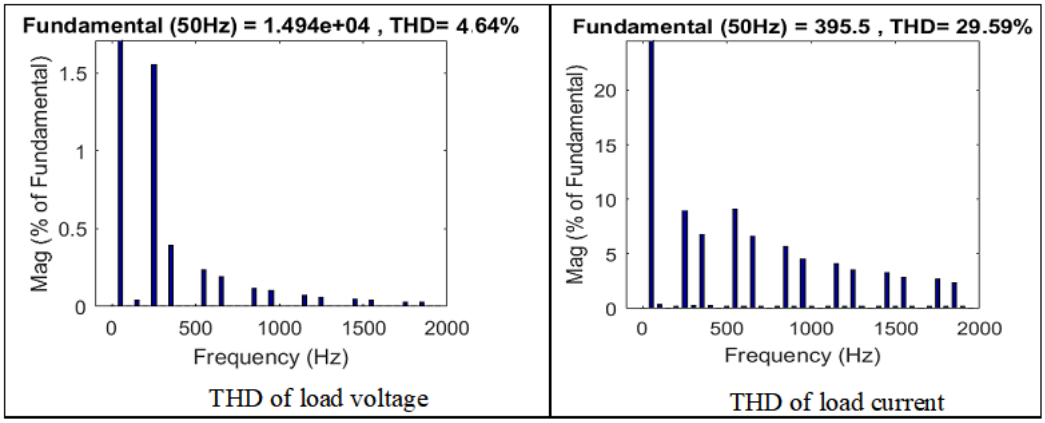

Figure 15 THD for load voltage and current profile for non-linear load under the contingencies.

5. Performance analysis of 5L-NPC-MLI-UPQC

The conventional 2L converters are well suited for low rating applications, but while working with high voltages, losses increases. Also switching losses ae well as Electro-magnetic interference (EMI) with voltage saturation across the switches are some of its draw backs. To improve the performance of the UPQC this research presents the MLI based UPQC converter topology (MLI-UPQC) [23]. MLI-UPQC can not only performs all the functions of conventional 2L-UPQC in-addition it increases the fault ride through capability of converter during system transients [24]. Also, it has reduced switching losses and frequency hence less EMI. The d-q theory control based on SRF is used to improve the dynamic performance during various operating conditions.

The topology of 5-Level NPC-MLI is designed using eight semiconductor-switches per phase, having 4-switches for positive cycle and another 4-switches for negative cycle, therefore 24-switches are required for three-phase system. In this work IGBT is used which is clamped at mid-point using 6-diodes. Voltage across each switch is distributed using capacitors C1-C4.

In the proposed work UPQC in addition of mitigating PQ problem like harmonic suppression, voltage regulation and reactive power compensation, also reduces the active and reactive power requirement for converters. The conventional topology for 5-level three phase NPC-MLI (5L-3Φ-NPC-MLI) requires in total 12 capacitances, four for each phase. In this work modified topology for 5L-3Φ-NPC-MLI is presented, in which the capacitances are reduced to 4 units by coupling all the three arms of the 5L-3Φ-NPC-MLI at the common nodes. The NPC topology suffers from the capacitance voltage balance. If the voltage across capacitors is not balanced the losses will be increased and the output waveforms will contain high harmonics. In literature, numerous topologies are developed to resolve this issue. [25] uses virtually optimized space vector concept, while [26] uses adjustable hybrid proportional space vector modulation technique. In literature, use of an extra rectifiers to keep the capacitance dc-voltage balanced is also mentioned [27]. All these techniques are complex and increases the system cost. In this work sinusoidal carrier wave modulation technique is used.

The Schematic diagram of the proposed 5L-NPC-MLI-UPQC is shown in figure 15. V_c is the voltage across coupling-transformer, V_S is the voltage of the grid bus, V_L is the voltage across the load bus, Z_L is the load impedance, V_{Sabc} is the three-phase reference signal of source voltage fed to the control unit. V_{DC} is the voltage across DC-link capacitor. For designing inverter control, V_{Sabc} is first transformed into abc to dq0 for simplifying the control design. A V_{abc_ref} is a 3-Φ reference voltage which is used to obtain a constant reference signal. PLL is used to calculate the phase angle and frequency. PI controller is used to design the reference sin signal which is than act as a carrier sine wave for SPWM generation. For designing SPWM, triangular pulses are generated using repeating sequence generator block of MATLAB which is than combined with reference sine wave and compared with relational operator to obtain gate pulses for power switches in NPC.

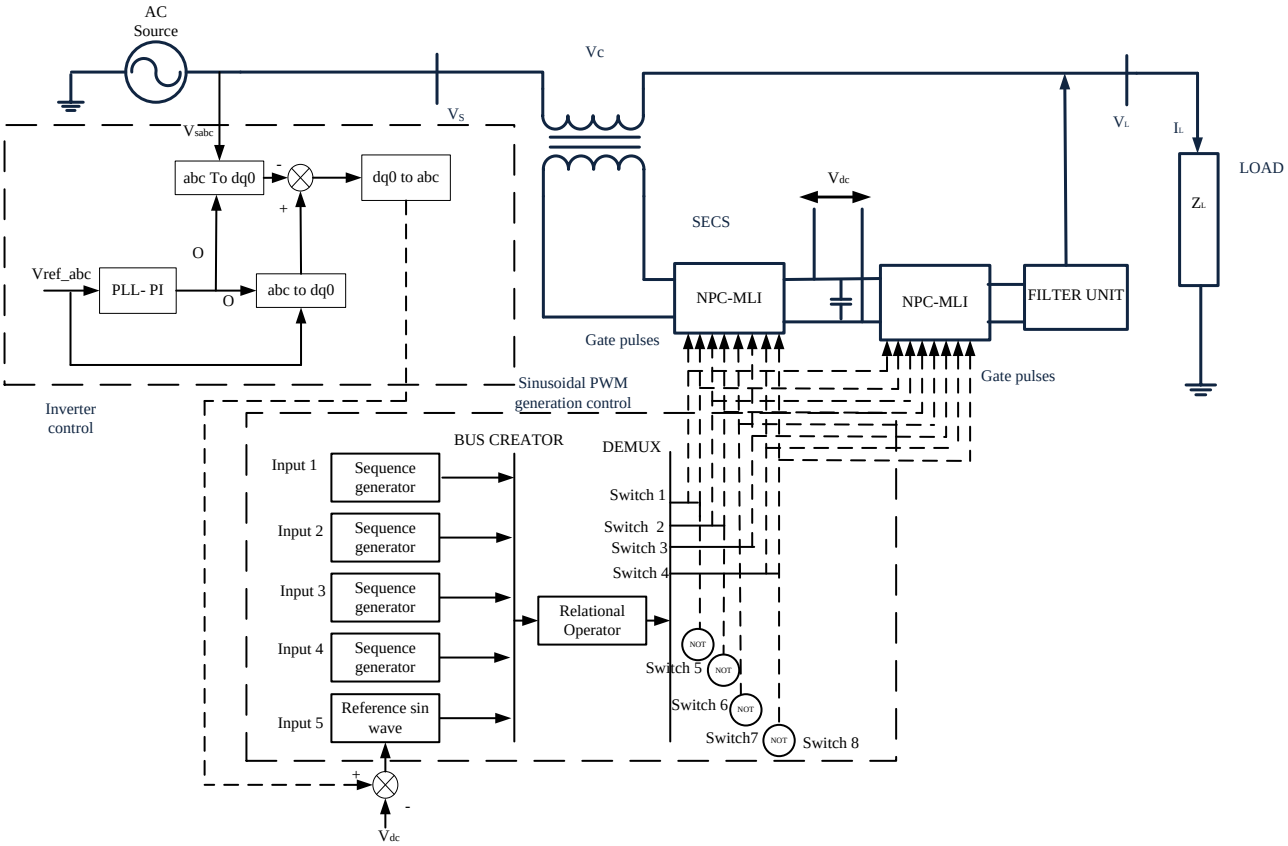

Figure 16. Simplified schematic diagram of proposed 5L-NPC-MLI-UPQC with control architecture.

The output of 5L-NPC three phase converter is in the form of stairs as presented by figure 17. The sinusoidal output is obtained by connecting the RL-RC filter unit at the output terminal of shunt converter. The operation of proposed 5L-NPC-MLI–UPQC under linear loading is perfectly synchronized and sinusoidal with load voltage and current as obtained in figure 17 with active and reactive power flow as shown in figure 18 and the power factor is 0.97 PU. The active power at the load bus is measured about 160 kW whereas reactive power in 8kVA. The THD graph at load-side for voltage and current is shown in figure 19 with load voltage THD of 1.05 % and that for load current is 2.49%. When operated under the heavy non-linear load of 8KW with simultaneous 150 kW, 1kVA inductive linear load injection at 0.2 sec. high harmonics currents are drawn by the load also the source undergoes sever fluctuations with three-phase to ground fault (TPGF) as shown in figure 12. The proposed topology mitigates the harmonics in source currents and also load currents THDs reduced as shown in Figure 21 and figure 22. The UPQC is connected between load and source bus, the fault at source side does not affect the load voltages and current. Hence when fault occurs at source side, the load voltages and currents are kept constant with perfectly synchronized and sinusoidal constant load profile. The 5L-NPC-MLI-UPQC have completely mitigated problem of symmetrical TPGF occurs at source side and maintains the load voltage and current to the normal operating condition as shown in waveforms of figure 20. The proposed UPQC tries to retain the stability at all operating conditions also the reactive power demand by the proposed 5L-NPC-UPQC is just 1.2 MVA which is discussed in detail in the next section.

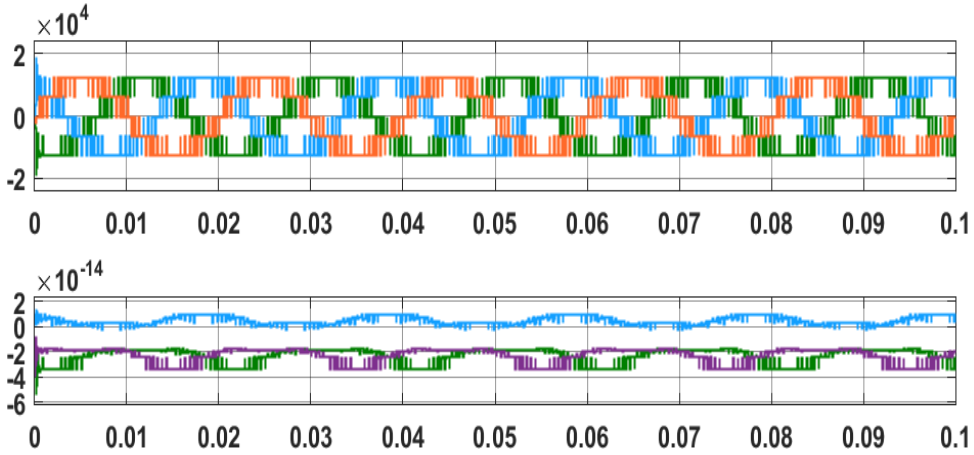

Figure 17. Output across the 5L-3Φ-NPC-MLI.

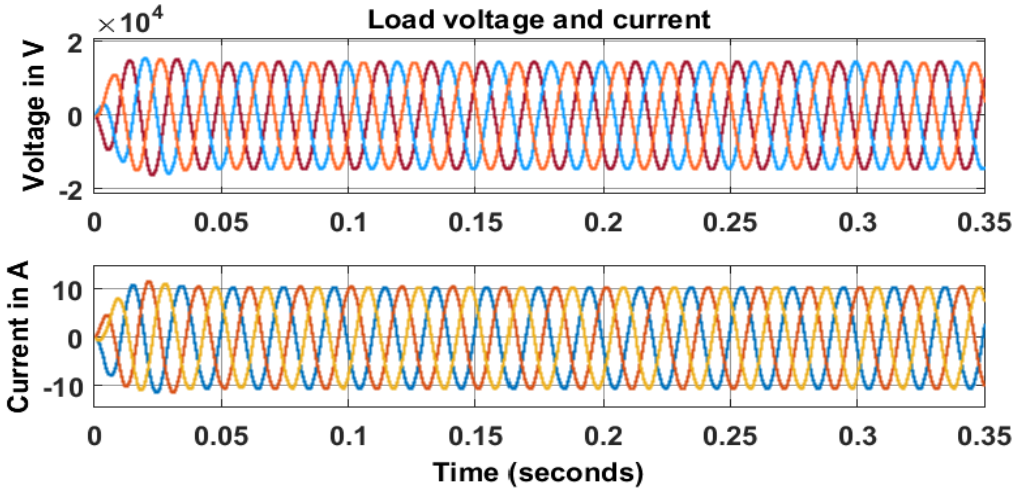

Figure 18. Load side voltage and current for linear loading with 5L-NPC-MLI-UPQC.

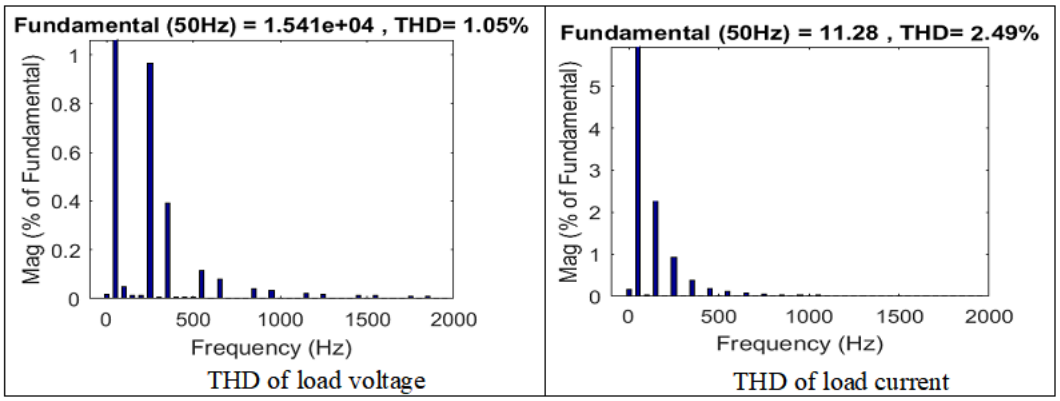

Figure 19. THD for load voltage and load current for linear loading with 5L-NPC-MLI-UPQC.

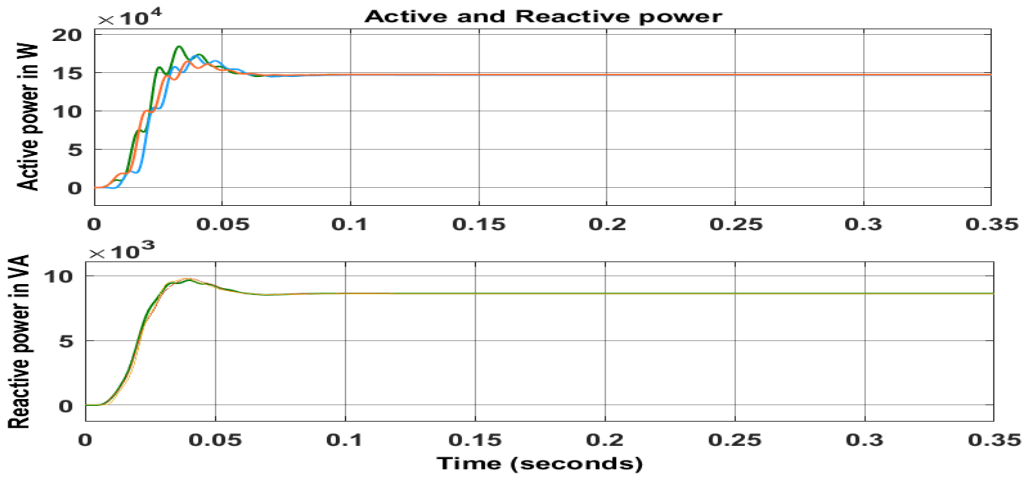

Figure 20. Active and reactive power for linear load under normal mode of 5L- NPC-MLI-UPQC.

Figure 21. Power factor for linear load at load bus with 5L-NPC-MLI-UPQC.

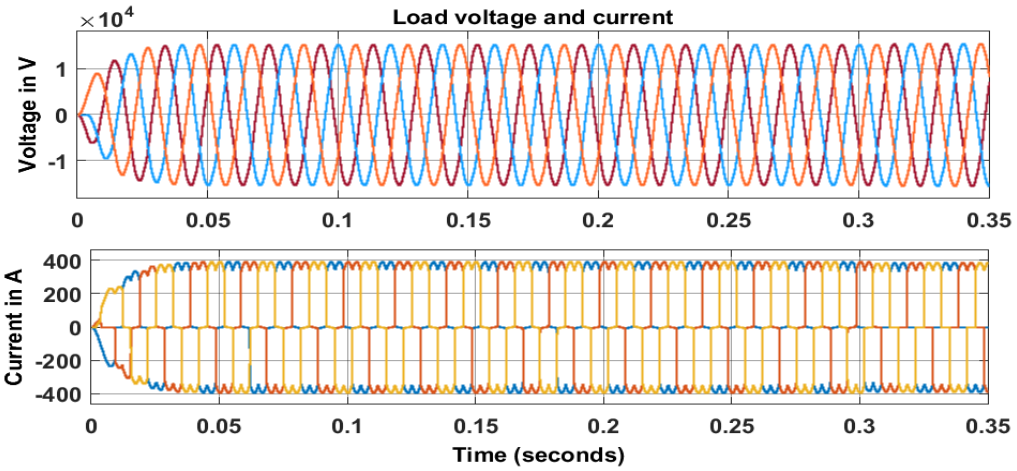

Figure 22 Load profile for non-linear load under the contingencies with 5L-NPC-MLI-UPQC.

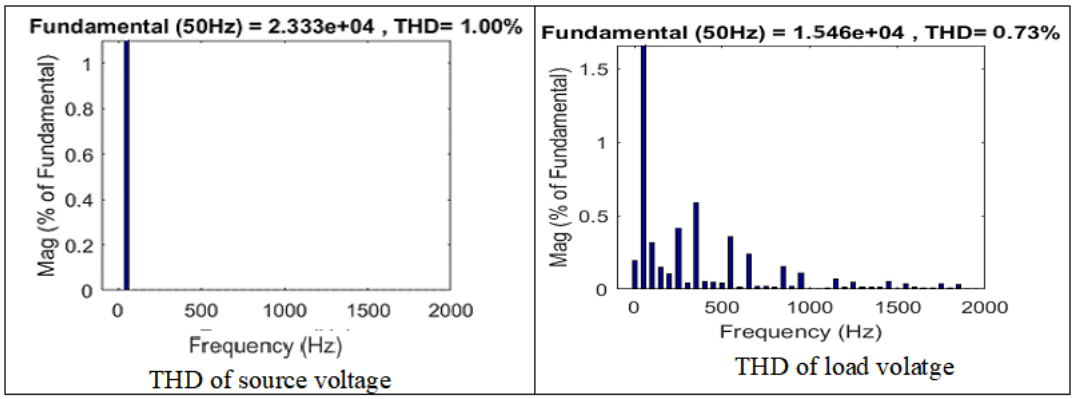

Figure 23. THD for source voltage and load voltage non-linear load under the contingencies using 5L-NPC-MLI-UPQC

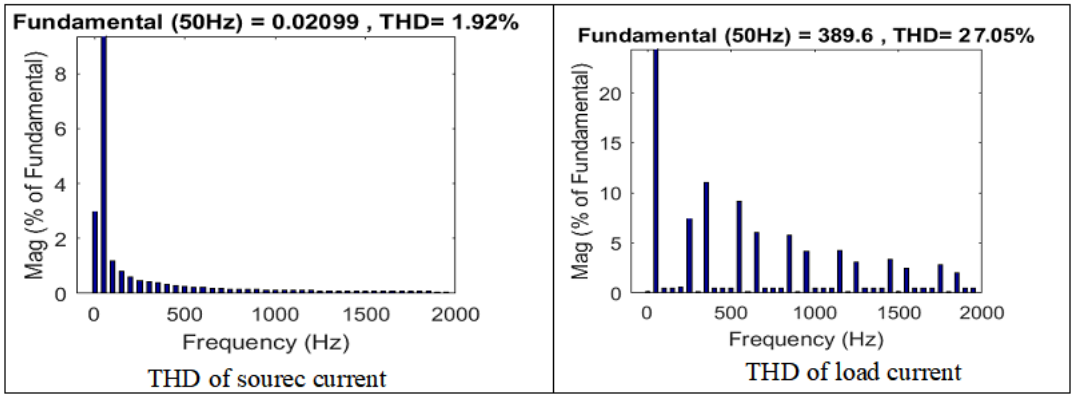

Figure 24. THD for source current and load current non-linear load under the contingencies using 5L-NPC-MLI-UPQC

6. Result discussion

The PE devices draws non-linear currents which adversely effects the Power Quality (PQ) of the system. Also, the intermittent nature of distributed generation system increases the problem of voltage instability as well as increase in harmonics both at grid side as well as load side is witnessed. These PQ issues if not rectified, may damage the voltage sensitive loads like, digital equipments, motor drives with variable frequency, programmable logic controllers, automated systems and processes, etc. UPQC presented in this work can achieve superior control over several PQ problems simultaneously. In the early stage of development of UPQC it was designed with conventional VSC, which can compensate for load as well as source harmonics simultaneously and also can mitigate the problem of voltage sag. But UPQC with conventional VSC topology is not efficient to compensate the harmonics completely also it draws high reactive power from the system as well losses are increased at higher switching frequencies as shown in figure 25. In the proposed work MLI-UPQC with modified NPC structure is presented which reduces harmonics as well as losses are reduced with power factor of about 0.97 PU as shown in figure 27 while power factor of source side is too low as shown in figure 26. The comparative analysis between conventional 2L-UPQC and 5L-NPC-MLI-UPQC is presented in table-2.

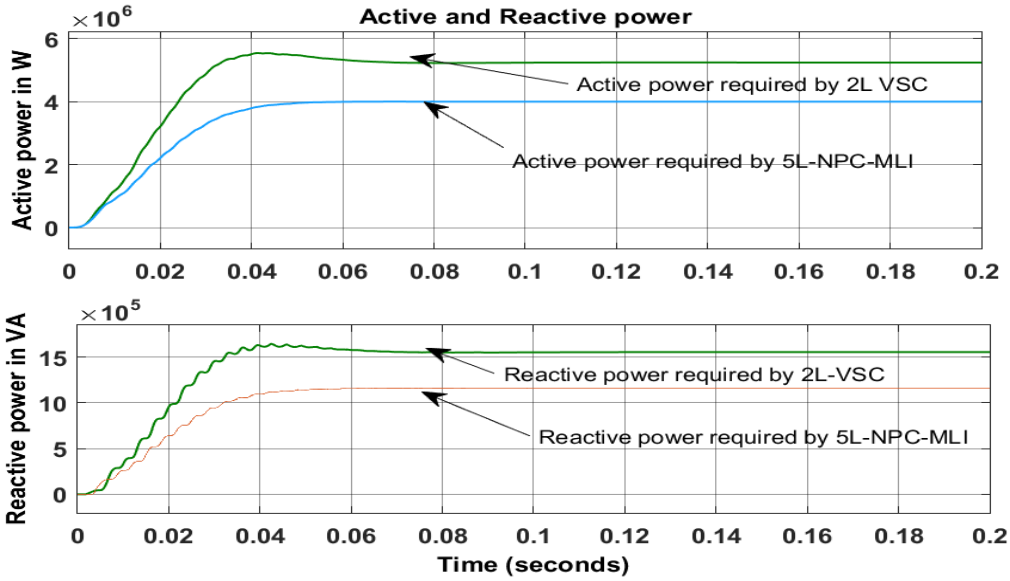

Figure 25. Active and reactive power requirement comparison of converters for 2L-UPQC and 5L-NPC-MLI-UPQC.

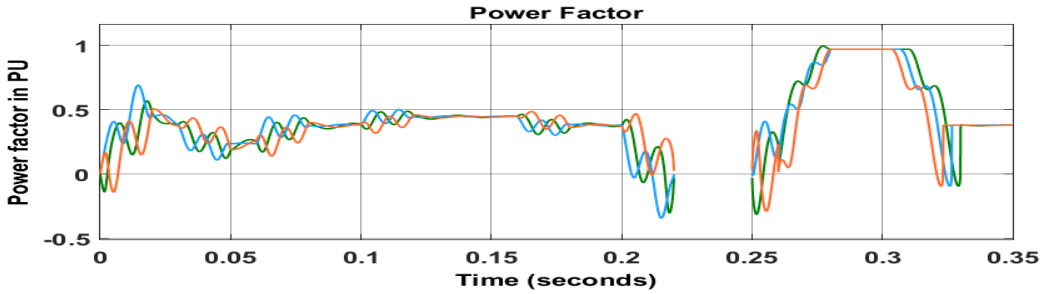

Figure 26. Power factor at source side for non-linear load under the contingencies.

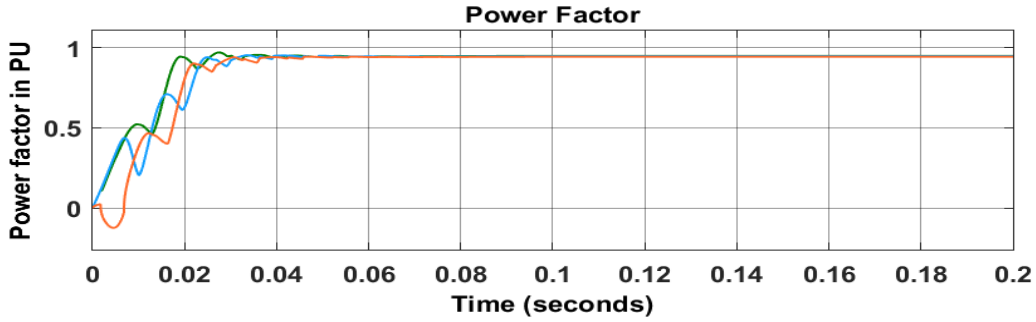

Figure 27. Power factor at load side for non-linear load under the contingencies using 5L-NPC-MLI-UPQC

Table 2. Comparative analysis for non-linear load under the contingencies using 2L-VSC-UPQC and 5L-NPC-MLI-UPQC

Topology	Source voltage THD %	Load voltage THD %	Source current THD %	Load current THD %	Active power	Reactive power
2L-VSC-UPQC	9.33	4.64	3.45	29.5	5 MW	1.5 MVA
5L-NPC-MLI UPQC	1.0	0.73	1.92	27.05	4 MW	1.1 MVA

7. Conclusion

UPQC is the most reliable CPD to mitigate various PQ issues in CUS. The UPQC controller found increased applications now-a days and various topologies are available to address various PQ issues in CUS. This work also presents one such UPQC topology designed using NPC MLI topology. the conventional NPC has high suffered from the drawback of capacitor voltage balance across the switches of the inverter. In this paper a modified topology for NPC capacitor voltage balance is presented. The capacitors for three phase 5L NPC forms a common node and sinusoidal carrier wave modulation is used to balance the voltage across each switch. The results are presented for sever voltage fluctuations at source side with three-phase fault. The comparative results are presented for converters with two topologies; one is conventional VSC and another is modified NPC-MLI based UPQC. The designed NPC-MLI-UPQC efficiently mitigates all the PQ issues in modern power system. NPC-MLI based converter plays a very important role by generating sinusoidal-synchronized output at inverter end with low THD content. Moreover, it could be easily extended to higher voltage level. It can simultaneously compensates load as well as source abnormalities both in current and voltage profile with the help of dual-converter control strategy. The proposed system provides the auspicious way out to most of the distribution system PQ issues and can be applied to DG and microgrid systems.

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