International Journal of Computing and Digital Systems
ISSN (2210-142X)
Int. J. Com. Dig. Sys. #, No.# (Mon-20..)

Design and Implementation of an Advanced Digital Communication System Based on SDR

Sadeem W. Al-saegh,[1], Mohamad A. Ahmed [2], Mahmod A. Al-zubaidy[3] and Abdullah B. Al-Qazzaz[4]

[1] *Communication Engineering, Mosul, Iraq*
[2] *Communication Engineering, Mosul, Iraq*
[3] *Communication Engineering, Mosul, Iraq*
[4] *Communication Engineering, Mosul, Iraq*

E-mail address: sadim.muhammad2018@stu.uoninevah.edu.iq, mohamad.alhabbar@uoninevah.edu.iq, mahmod.mahmod@uoninevah.edu.iq, abdullah.hazem2018@stu.uoninevah.edu.iq

Received ## Mon. 20##, Revised ## Mon. 20##, Accepted ## Mon. 20##, Published ## Mon. 20##

Abstract: Simplicity, flexibility, and high scalability are mandatory for modern digital communication systems. This can be achieved using software-defined radio (SDR) technology, which depends on digital signal processing (DSP) software algorithms. This paper considers designing the modulation and the demodulation parts of a single carrier digital communication system based on a Microcontroller(MC),, in which the signal is modulated digitally using a look-up table (LUT) module, while the receiver demodulates the signal using a digital signal processing algorithm by utilizing a single carrier discrete Fourier transform (DFT), both the receiver and transmitter employ Teensy 4.0 microcontroller which can be programmed using C++ language. The target data rate that will be used as a test for this paper is 10 kilo symbols/sec (KS/s), and it will support multi-modulation types. For the transmitter, modulation schemes such as BPSK, QPSK, 8QAM, 8PSK, and 16QAM are generated, while at the receiver, the symbols phases are exploited to detect the signal, rather than the amplitude, and this method is suitable for any type of modulation schemes, as a summary in this paper will achieve the design of two new ideas first is modulate the signal using MC and the other is the method of demodulate the signal using the MC.

Keywords: Digital modulation, microcontroller, software-defined radio (SDR), C++, Mary phase shift keying (MPSK), and M-ary Quadrature amplitude modulation (MQAM).

1. INTRODUCTION

Digital modulation technologies are very important in modern communication systems. In the last years, the world has seen a huge expansion in this field, Digital modulation took the place of analog modulation types in many communication systems, which in the previous year's wide development in the digital communication field has been done.

The world has seen in the last era a large industrial revolution in microprocessors and Digital Signal Processing (DSP) algorithms which makes the microprocessor year by year more suitable to be employed in the field of DSP and most digital communication systems.

Nowadays, flexibility and scalability become prerequisites in modern communication systems because of the new bands of spectrum and the evolution of communication systems that we use. For these reasons, communication systems become dependent on a fixable

E-mail:author's email

software system named software-defined radio (SDR) technology, which is employed for modulation and demodulation with the assistance of the DSP algorithm, compared to the use of these techniques in the past for a fixed unique circuit for every modulation system, This technology made the way to develop an updated modern digital communication system is easier [1].

In the SDR system, data is processed in a microprocessor and modulated digitally, then it is sent to a digital-to-analog converter (DAC) circuit to obtain the modulated signal. The latter is sent to the RF component, On the receiver side, the received signal is converted to digital using an analog-to-digital converter (ADC), which achieves processing using DSP in the microprocessor to demodulate the signal [1-3].

There are various SDR architectures and topologies, some topologies depend on FPGA and some on the General Purpose Processor (GPP), and there are also SDRs using both to obtain the advantage of GPP and FPGA, The choice depends on speed, price, and SDR working environment [4] and [5], However, the aim of this paper emphasizes the modulation and demodulation stages.

A real-time modulation scheme based on an FPGA for digital communication has been designed and implemented in [6–8], in which the FPGA is programmed by utilizing VHDL for the sake of obtaining higher performance and simpler confirmation, The disadvantage of the FPGA is it has lower flexibly and harder to implement than the GPP [1].

In this paper, the aim is to investigate the ability and the difficulty of designing a special digital modulation system using a microcontroller and attempt to implement the design. The microprocessor is utilized by using a clock of 600MHz with speed CORTEX M7, which is built in the MIMXRT1062 microcontroller chip, which is used then by the teensy 4.0 microcontroller programming board [9]. The board can be programmed using C++ language and Arduino IED. This microcontroller has been chosen because the clock speed is suitable for the DSP field, and its cost is low compared to other microcontrollers, also it has been used in the digital modulation field [10].

The main contribution of this paper is the design and implementation of multi real-time modulation types transmitter and the real-time demodulation of a single carrier by utilizing a Teensy 4.0 MC and DSP algorithms. The signal can be digitally modulated in different modulation schemes at the transmitter by utilizing a look-up table (LUT) module that stores all possible symbols for any modulation scheme in the microcontroller. On the other hand at the receiver, a digital signal processing algorithm, via utilizing a single carrier discrete Fourier transform (DFT), has been proposed and implemented. The detection by using the proposed method relies on phase detection of the symbols rather than the conventional amplitude detection. For perfect detection of the transmitted signal, synchronization, guard delay, and sensing methods are proposed to avoid interference.

2. Digital modulation

A. BPSK

BPSK is used to send one bit in every symbol with two-phase probabilities one phase for high level and another for low with 180^o differences, the mathematical expression can be defined for bipolar data bits as:

$$s_{BPSK}(t) = B(t) * \cos(w_C t) \quad (1)$$

Where B(t) is the data bits in bipolar form {1 , -1} and w_C is the radio frequency of the carrier, The BPSK has the lowest symbol error rate (SER) among all other digital modulation systems because it has only two phases[11], therefore, it is suitable for testing ,the most well-known digital communication system that use PSK modulation is the Global Positioning System(GPS)[12].

the consumed bandwidth for the BPSK is twice the bite rate which is higher than other M-ary PSK (MPSK) schemes, However, the two symbol will be calculate and store in the Random access memory (RAM) when the MC will start, this process will happen once and no need to calculate the signal for every symbol, and this method will be as well as every other modulation type that will be use.

B. Quadrature PSK (QPSK)

QPSK is utilized to transfer two bits per symbol with four-phase probabilities which can send the same bit rate of PSK with half symbol rate. This means it uses the half BW of PSK, the standard four-phase that QPSK uses is $45^o, 135^o, (225^o \; or \; -135^o), (315^0 \; or \; -45^o)$.

The QPSK waveform can be generated by taking two-bit every symbol and multiplying the first bit with a local oscillator, i.e. a single-tone sinusoidal signal, while the second bit is multiplied with the same sinusoidal signal but with 90^o phase shift. The two branched of the two bits are then summed to obtain the final QPSK waveform. Table 1 explains the final result of the QPSK transmitter circuit

TABLE .I Input-output of the QPSK transmitter

BIT0 B_0	**BIT1** B_1	$a = B_0 \sin(\theta)$	$b = B_1 \sin(\theta + 90)$	**a +b**	**Amp**
-1	-1	180°	270°	225°	$\sqrt{2}$
1	-1	0°	270°	315°	$\sqrt{2}$
-1	1	180°	90°	135°	$\sqrt{2}$
1	1	0°	90°	45°	$\sqrt{2}$

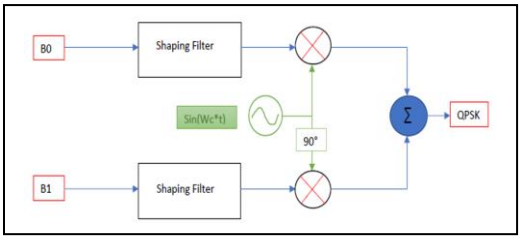

Figure 1. QPSK Trasmiter

$QPSK = B0(t)\sin(w_C t) + B1(t)\cos(w_C t)$ (2)

because the bits in bipolar form then I= $B0(t)$ and Q=B1(t), also this equation will be used to calculate the symbols form for the four cases and will stored in the RAM to give it as output according to the inputted bits.

At the receiver, the incoming signal is multiplied coherently in the two branched one for $sin(\theta)$, and the other with $sin(\theta + 90^o)$, at the output of the two mixers, the signals are filtered by passing through a low pass filter (LPF), and filtered signals must represent the I and Q values are compared with a reference voltage to decide the logic in each branch as shown in Fig.2.

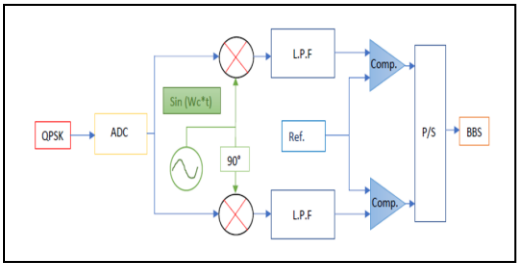

Figure 2. QPSK receiver

The most well-known communication system that use the QPSK modulation , is the Digital Video Broadcasting – Satellite (DVB-S) and DVB-S2.[13,14]

C. 8PSK

8PSK modulation scheme is employed to send 3 bit per symbol, which mean that it can send treble the data rate compared to the BPSK with the same bandwidth. This modulation scheme has 8 potential phases with $360^o/8 = 45^o$ phase differences between any two successive symbols. There are two common constellation diagrams for the 8PSK, the first constellation diagram has 8 symbols with 45 distances in angle, with these angles $\pm 22.5^o, \pm 67.5^o, \pm 112.5^o, \pm 157.5^o$ [15], [16] and for the other, the angles start from 0^o and end at $\pm 180^o$[15], however, every type has it's own I and Q values table to produce the signal with the require phase, in the receiver after the multiplication stage the result will be multiple levels of voltage for the I Q values, to decode these values and get the modulated data bits, multi comparator for every side must be use with a logic circuit or ADC can be also used, however for the methods of this paper all the demodulation stages will be block of code, *t*he most well known communication system that uses the 8PSK modulation, is the DVB-S2[14].

D. QAM

Quadrature Amplitude Modulation (QAM) sends the signal with a variation of amplitudes and phases. This scheme is used wildly in most modern digital communication systems because it can send a high number of bits per symbol with better BER compared to MPSK, the most well known communication system that use the QAM is the wireless local area network protocol for the Wi-Fi standers. [17]

The higher well known order has been used of QAM is 4096 [18], which means that it can transfer up to 12 bits per symbol, QAM need linear power amplifier because it use multiple levels of amplitude, rather than the nonlinear one which it is more efficient than the first one, to overcome this problem APSK(*Amplitude and phase-shift keying*) modulation can be use ,in this type also it use phase and amplitude for modulation but it use lower levels of amplitude [19], however, in this paper, the 8QAM and 16QAM are used at the transmitter only .

D. A. 8QAM

The 8QAM is usually used in optical communication [20], [21], and there are many designs of constellation diagrams as shown in the fig. below

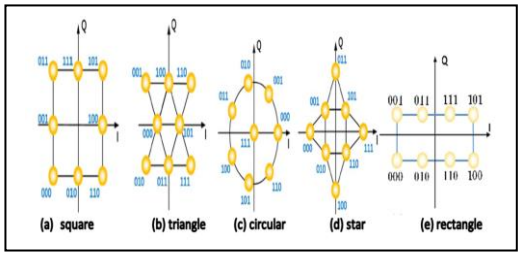

Figure 3. QAM constellation diagrams [21-23]

The square constellation diagram that is shown in Fig. 4 has been chosen for the transmitter part, this shape use the same phases that the 8PSK is use, from the properties of the square we can conclude that the four points that are in the corners of the square are 1.41 higher amplitude than the other four points, however the 8QAM consider

better than 8PSK by 1 DB .

D. B. 16QAM

16QAM send 4 bit per symbol with 12 probable phases and three amplitude levels as shown in Fig. 4 the constellation diagram and the time domain signal of the 16QAM, they were plot using a Matlab simulation also.

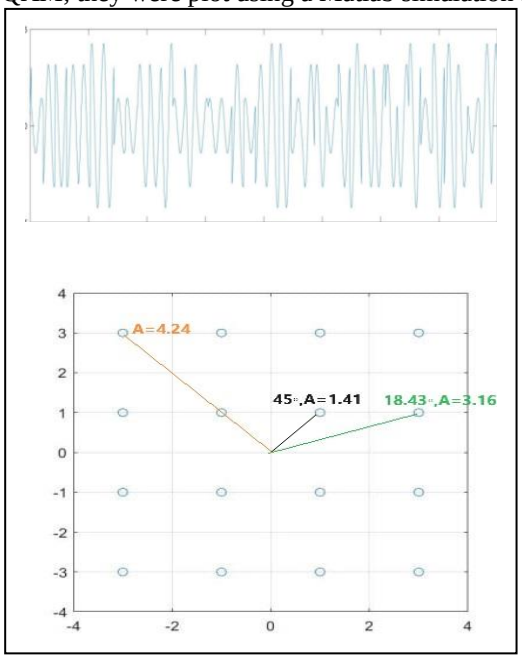

Figure 4. 16QAM a) time domain and b) constellation diagram.

as mentioned early there are three amplitude levels for the 16QAM signal 1.41, 3.16 and 4.24 , and 12 phase 18.43^o , 45^o , 63.43^o , 108.43^o ,135^o ,153.43^o , 180^o ,- 18.43^o ,- 45^o ,- 63.43^o , -108.43^o ,-135^o and -153.43^o 16 QAM use in different communications system like Digital Video Broadcasting – Terrestrial (DVB-T) , Wi-Fi 802.11n stander and Digital subscriber line (DSL) [24-26] ,16QAM has higher BW efficient than other previse types, which it can transfer four times of data rate of the PSK with the same band width, however for the design of this paper for the transmitter, the 16 possible waves of the 16QAM will be generated and stored in the MC.

3. SDR

Most modern communication systems rely on SDR technology which can offer flexibility and low cost, the main idea is that the signal is converted to digital form using DAC and then processes the signal using DSP, the SDR receiver may contain an analog downconverter RF stage before the DSP processing, this stage may be not exited some models, in which the latter model employs direct sampling.

SDR provide maximum flexibility for the digital communication system especially when it use GPP, because it is allow the same headwear to be use with different air interface standers and the system could be easily update by only update the software part [27], one example for SDR system is the general purpose SDR type like RTL dongle receiver which it can be used for researching and analysis the frequency spectrum.

Also SDR can be combined with artificial intelligence (AI) to signal to process, offering innovative solutions for improved intelligence gathering and analysis, with significant current capabilities and potential future advancements [28-30].

For the transmitter, the data can be modulated digitally and delivered to DAC to convert it to a real signal, the modulated signal is then passed to the RF component to be ready for transmission.

4. DESIGN IMPLEMENTATION

A. Transmitter

To produce the modulation signal using the microcontroller, a DAC circuit must be used, R-2R ladder DAC circuit has been chosen to use because it is simplicity with suitable performance without needing a complex filter circuit, and R-2R content of only resistors, the design is shown in the Fig. 5

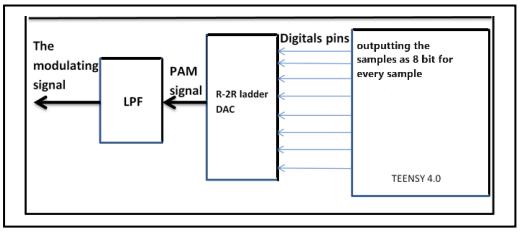

Figure 5. R-2R DAC.

The R-2R is a parallel DAC and in this design it work with 8-bit resolution for every sample which mean the step level will be 1/255 V the output of the DAC will be zero order hold (ZOH) signal. The samples of the signal are generated and stored digitally by a look-up table (LUT) module inside the microcontroller for every modulation type. Each symbol has 25 samples as assumed in this paper , so it is easier to shape the signal using the LPF, the frequency or symbol rate can be

control by the controlling the delay between the samples which can be calculate as following.

$$delay\ btween\ samples = \frac{T_{sy}}{N_s} \quad (3)$$

Which $T_{sy}$is the duration of the require symbol rate and $N_s\ is\ the\ nuber\ of\ samples$, and there many way to produce the delay for the MC but the most accurate method is to use the clock counter number inside the teensy, which every clock cycles take $\frac{1}{600MHz\ clock\ speed}$=1.67ns. (4)

As a result of the first try on the breadboard, 10 Kilo symbol per second (KS/s) of the different modulation signal are modulated successfully with high resolution in the real-time as shown in Fig. 6 , which it contain a collection of the results for the multi modulation signals in time domain using the oscilloscope in the lab of the college, noting that all modulation were based on sin signal not cos, in other word 90 degrees rotation has been used for the Fourier transform, because the phase can be represent easer for the sin signal which it start from 0 degrees .

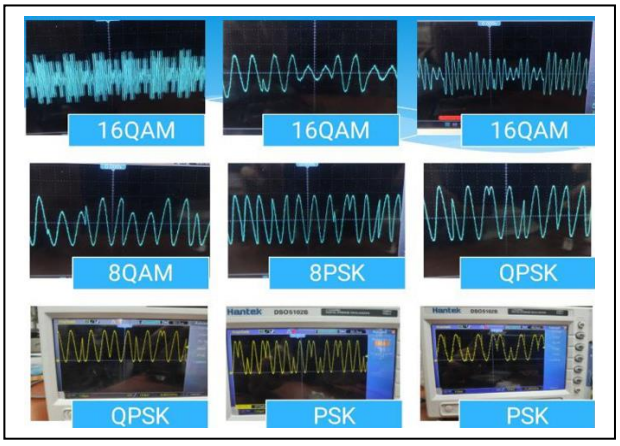

Figure 6. Signals Produced at the Transmitter.

Also the bandwidth of the modulation has been calculated using the FFT property in the math option of the oscilloscope and these results are perfectly consistent with the theoretical formulas of the BW measuring ,however by sending the same symbols rate like 10ks/s using different modulation types, in this situation the bandwidth will always be the same, for that reason different symbol rate has been used, and Fig. 7 show the bandwidth need to transmit 10KBit/s using PSK and QPSK modulation, for PSK with 10KS/s the bandwidth is 20 KHZ and for the QPSK with 5 KS/s the bandwidth is 10Khz.

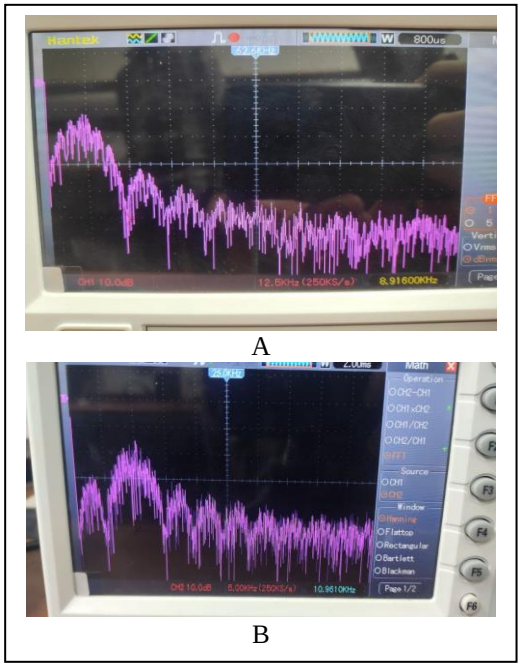

Figure 7. a) PSK frequency domain b) QPSK frequency domain

The filtering circuit design for the signal was easy and smooth with simple first order low pass filter the reason was because the high number of samples per symbol has been used, in Fig.8 show that different in the signal shape for PSK modulation before and after the low pass filter.

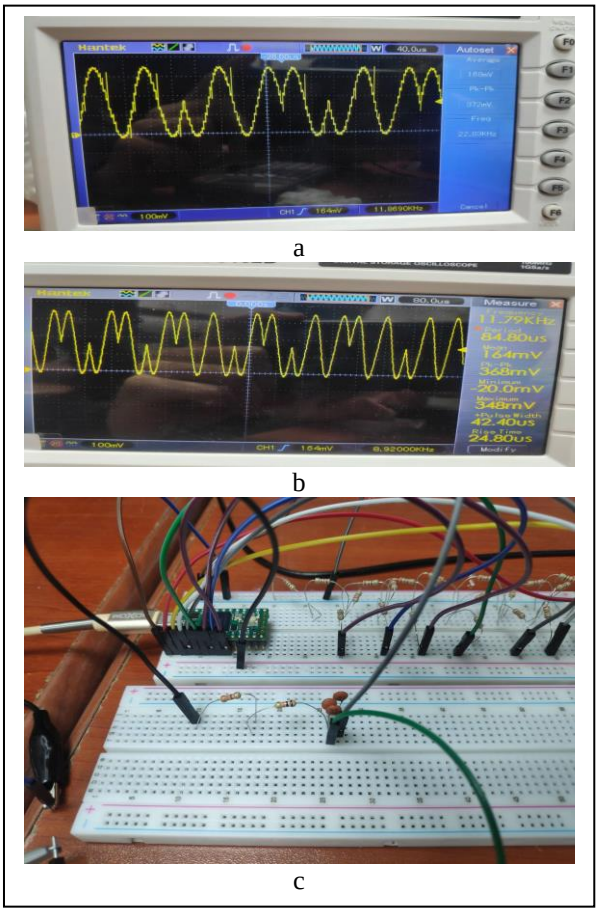

Figure 8. a) DAC output b) filter output c) transmitter

After these results a PCB board has been design for the transmitter circuit to make it more suitable for testing environment and also as a lab board, the final design of the transmitter is shown in Fig. 9

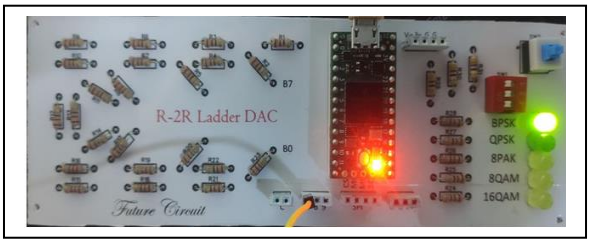

Figure 9. PCB of the designed system.

From this figure, it can be noticed that additional components have been added in addition to the MC and DAC, such as LEDs and switches for the selection of the required modulation scheme and some serial peripheral interface (SPI) to make the measurement and testing of the designed system more convenient. The maximum symbol rate obtained for the 25 samples per symbol using the Teensy is about 400kS/s.

B. Receiver

the receiver teensy MC will take four samples per symbol with fix delay between samples from the analog digital modulation signal, using the internal ADC with 8 bits as resolution as shown in the fig ,and the delay can be calculate as

$$T_s = \frac{T_{se}}{4} - T_{ADC} \quad (4)$$

Which T_{ADC} is the time need to get one sample and for this case it is equal to 2.4us

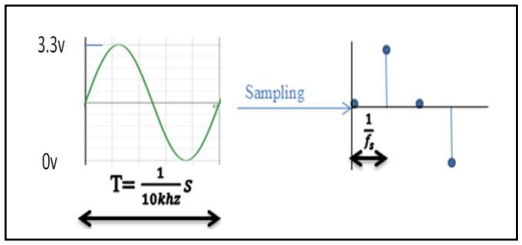

Figure 10. Synchronization method

the four samples for every symbol must be process using SC-DFT as the following

DFT=

$$\sum_{n=0}^{n=N-1} S(n) * e^{\frac{-i2\pi kn}{N}} \quad (5)$$

For single carrier and 4 samples it will be

$$\sum_{n=0}^{n=3} S(n) * e^{\frac{-i2\pi n}{4}} \quad (6)$$

which

$$e^{-jx} = \cos(x) - jsin(x) \quad (7)$$

then

$$DFT = \sum_{n=0}^{n=3} S(n) * \left(\cos\left(\frac{i2\pi n}{4}\right) - jsin\left(\frac{i2\pi n}{4}\right)\right) \quad (8)$$

The result will be an complex number

$$DFT = I + jQ \quad (9)$$

Now we can use $\tan^{-1}$ to find the phase of the signal

$$\text{phase} = \tan^{-1}\frac{Q}{I} \quad (10)$$

But $\tan^{-1}$ give the phase with the range of $-\frac{\pi}{2}$ *to* $\frac{\pi}{2}$ only so we need to add additional parts to the code to find the phase or we can use atan2 function instead, however because the sin is used as a reference for this paper to the x axes then DFT equation must be changes to be suitable with it , first the x axis become represent the sin and the y axis represent the cos and the negative sign of the y axis

convert to positive , and that represent 90 degrees of rotation to the x-y plane, the equation is shown below.

$$DFT = \sum_{n=0}^{n=3} S(n) * (\sin\left(\frac{i2\pi n}{4}\right) + jcos\left(\frac{i2\pi n}{4}\right)) \quad (11)$$

The main challenge is how to keep synchronization inside the microcontroller for perfect signal recovery by exact estimation of the phase. To overcome this issue a synchronous symbol has been added at the start of the transmission so the receiver can know the start point of the first symbol by sensing the change in the channel and start to take samples in the correct position, the synchronous symbol can be a DC signal or a cos signal as shown in Fig. 11.

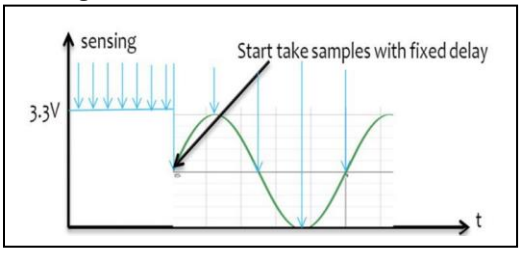

Figure 11. Sampling process explanation

However, the delay between the expected and the actual samples is not perfect in each symbol due to a shift introduced in the sample position, which leads to an error in the detection of the phase after several symbols as shown in Fig. 12.

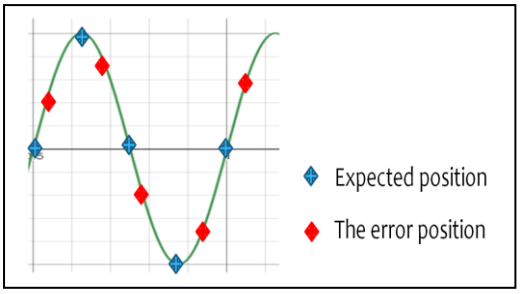

Figure 12. Sample shifting

To overcome this issue, symbol synchronous must be applied after a particular number of symbols as shown in Fig. 13.

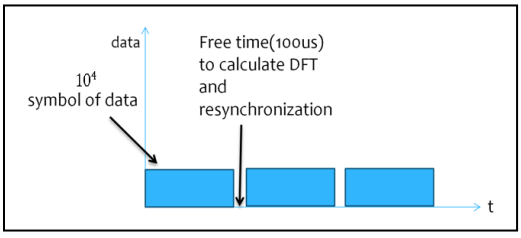

Figure 13. Resynchronization

The processing of the signal at the receiver is illustrated in Fig. 14, which shows the implemented steps in a flow diagram.

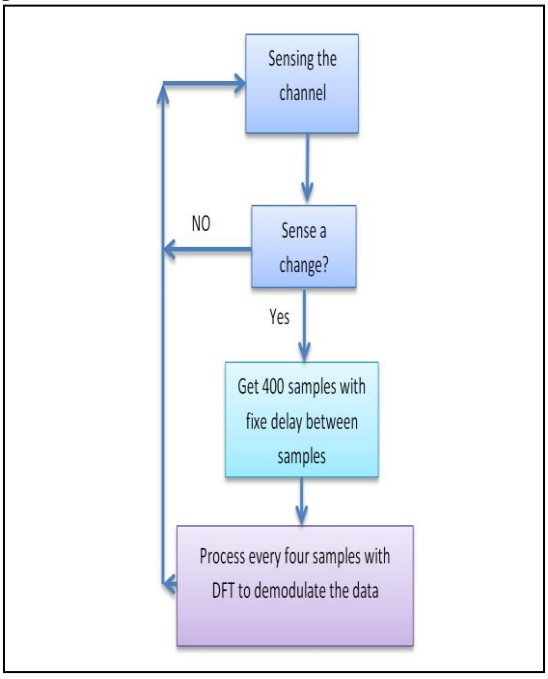

Figure 14. Receiver flow diagram

After adding all the required modifications to the receiver on MC, synchronization is achieved and the designed receiver demodulates successfully the PSK, QPSK, and 8PSK signals with 10KS/s.

However, the 8PSK was not suitable with the 8-bit, i.e. byte size, and the 8PSK transfers 3 bits per symbol, so it needs an additional block in the code to select 3 bits for each symbol instead of an even number of bits for other modulation schemes.

5. RESULT ANALYSIS

As shown in Fig. 15 after the data was demodulated and stored in the Teensy of the receiver, it was printed on the screen using a serial USP port and serial monitor tool that the Arduino IED offers. The data rate of one carrier of 10 Kilo symbol per second (KSps) is obtained as 10kbit for PSK, 20kbit for QPSK, and 30kbit for 8PSK. Furthermore, the modulation type can be changed for both the transmitted and the receiver.

Figure 15. Demodulated data

Moreover, from the experience the transmitter can reach a speed of up to 400 Ks/s, when 16QAM is chosen. For this modulation scheme, the system can transmit up to 400KS/s*4bits=1.6Mbps, and the frequency can increase by decreasing the number of samples per period, which is assumed 25 samples per period in the proposed design. This makes the LPF design much easier with lower complexity. Additionally, the data rate can be increased using a multi-carrier system, and the receiver speed can be increased by taking three samples per symbol instead of four.

The receiver needs about 70us to implement the DFT for the 100 symbol, and the internal ADC of Teensy 4.0 needs 2.4us for every sample at a maximum rate of 417 KS/s, which theoretically can demodulate signals up to 100KHz by using this method if four samples per symbol are considered, not three per symbol, but the synchronization still needs an additional symbols duration.

The maximum available frequency is 100 kHz, and the period of one symbol is t=1/100 kHz =10us. Thus, DFT needs 70us for processing plus 30us as a guard interval which means that 100us is required for processing 100 symbols, i.e. the processing time is equal to the time intervals of 10 symbols.

Therefore, the number of symbols needed for processing is 100us/10us=10symbol for every 100 symbols of data, from these results, we can conclude that the maximum symbol rate that can be obtained from the designed system is $100KSps - (100KSps/100 * 10) = 90KSps$ of data.

It is noteworthy that the receiver speed can be increased by adding an external ADC, however, this data rate is more than the real-time digital voice needed. This method of synchronization of the symbol can be applied also to a multi-carrier system like OFDM which we will need only to synchronize the symbol's length not all the subcarriers.

Conclusion

MC makes the design of digital communication system flexibility but limited with the range of the clock speed of the processor, the design can be changed according to the requirement of the systems and applications. This paper has considered designing multi real time modulator for single carrier based on a MC. The signal is digitally modulated over different modulation schemes at the transmitter by utilizing an LUT model that stores all probable symbols of any modulation scheme in the Teensy microcontroller. On the other hand at the receiver, a DSP algorithm, via utilizing a single carrier discrete Fourier transform (DFT), has been proposed and implemented. The detection by using the proposed method relies on phase detection of the symbols , and it successfully modulates the data of 10ks/s, because of the flexibility of the MC a synchronous symbol has been added to the signal to confirm the correct demodulation. There are a wide number of ideas that can be applied for this project in which, the transmitter can be used as a lab board or a flexible real-time transmitter for signal carriers or multi-carrier systems like OFDM with 400kS/s speed, and for the receiver, it can use with speed can be suitable for real-time digital voice, the maximum assumption speed was 90Ks/s for four samples per symbols with ability of change to multi modulation types, the ability of implement QAM signal to the receiver can be investigated, the design with the transmitter and receiver can be use also as half-duplex connection with multiple devices, also can apply the multi-carrier system like OFDM or make it automatically discover the bit rate and the type of modulation also it can work as a two-way communication half duplex. Moreover, this microcontroller with the 600MHz clock speed can handle a maximum data rate that can be suitable for real-time digital voice.

ACKNOWLEDGMENT

REFERENCES

[1] Wyglinski, A. M., & Pu, D. (2013). *Digital communication systems engineering with software-defined radio*. Artech Houe.

[2] L. Frenzel, Principles of electronic communication systems. McGraw-Hill, Inc., 2007.

[3] J. R. Machado-Fernández," Software Defined Radio: Basic Principles and Applications", DOAJ, vol. 24 , no. 38 , pp. 79-96 , 2014

[4] J. T. Curran, C. Fern´andez-Prades, A. Morrison, and M. Bavaro, "Innovation: The continued evolution of the gnss 8 software-defined radio," GPS World, vol. 29, no. 1, pp. 43–49, 2018

[5] *R. Akeela and B. Dezfouli, "Software-defined radios: Architecture, state-of-the-art, and challenges," Computer 14 Communications, vol. 128, pp. 106–125, 2018.* Rami Akeela and Behnam Dezfouli, "Software-defined Radios: Architecture, state-of-the-art, and challenges", Computer Communications, vol. 128, pp. 106 125, 2018.

[6] G. AL Zubaidy, Qaddoori, "Efficient design and implmmentation of the realtime multi types digital modulations 16 system bassd fpga," Engineering Science and Technology, vol. 18, pp. 974–989, 2023.

[7] N. Gadawe and M. Al Zubaidy, "A new method for hardware implementation of digital modulator system on fpga," 18 The Mediterranean Journal of Computers and Networks, vol. 6, no. 2, p. 81, 2010.

[8] Joyashree Bag, Subhashis Roy, P. K. Dutta And Subir Kumar Sarkar, "Design of a DPSK Modem Using CORDIC Algorithm and Its FPGA Implementation", IETE, Vol. 60, no. 5 ,pp. 355-363, 2014.

[9] J.Lewis, "Teensy 4.0 Brings 600 MHz Cortex-M7 to the Arduino World", hackster.io, 2019, Available: https://www.hackster.io/news/teensy-4-0-brings-600-mhz-cortex-m7-to-the-arduino-world-13d451477918

[10] C. Xia, "A low-cost modular underwater acoustic communication system," Ph.D. dissertation, Massachusetts 22 Institute of Technology, 2020

[11] Kattoush, A. (2005). Digital communications. Amman: Dar Al-Manahej For Publishing & Distribution

[12] Liu, Haochen. "BPSK/BOC Modulation Signal System for GPS Satellite Navigation Signals." *Journal of Physics: Conference Series*. Vol. 2384. No. 1. IOP Publishing, 2022.

[13] Elbert, Bruce. The Satellite Communication Ground Segment and Earth Station Handbook., UK , Artech House,2014.

[14] Ilcev, Stojce Dimov, Global Mobile Satellite Communications Applications: For Maritime, Land and Aeronautical Applications Volume 2, Germany, Springer International Publishing, 2017.

[15] Mehta, R., & Lobiyal, D. K. (2017, July). Energy optimization in ad-hoc networks with MQAM, MFSK, MPSK and MPAM modulations. In *2017 8th International Conference on Computing, Communication and Networking Technologies (ICCCNT)* (pp. 1-5). IEEE.

[16] R. Caballero, "8psk signaling over non-linear satellite channels." International Foundation for Telemetering, 1996

[17] A. Yarali . From 5G to 6G: Technologies, Architecture, AI, and Security, UK, Wiley, 2023.

[18] V. Camarchia, "Electronics for Microwave Backhaul", USA, Artech House Publishers ,2016.

[19] P. Timothy, and A. Jeremy E. Satellite Communications, UK , Wiley , 2019.

[20] Guo- Wei Lu, José Manuel Delgado Mendinueta, Takahide Sakamoto, Naoya Wada, and Tetsuya Kawanishi, "Optical 8QAM and 8PSK synthesis by cascading arbitrary 2QAM with squared QPSK", *Optics Express*, vol.23, no. 16, 21366-21374, 2015.

[21] J.Zhao, C.Qin, M.Zhang, and N.Chi, "Investigation on performance of special-shaped 8-quadrature amplitude modulation constellations applied in visible light communication", Photonics Research, vol. 4, no. 6, pp. 249-256, 2016.

[22] P.Zou, Y.Liu, F.Wang, N.Chi. (26–29 October 2018), "Mitigating Nonlinearity Characteristics of Gray-Coding Square 8QAM in Underwater VLC system", Asia Communications and Photonics Conference 2018 (ACP), Hangzhou China[Online] Available: https://opg.optica.org/abstract.cfm?uri=ACPC-2018-Su4D.3

[23] M. A. Taufiqurrahman, I. G. P. Astawa, and A. Sudarsono, "Performance analysis of circular 8-qam constellation 33 with mmse equalizer for ofdm system using usrp," EMITTER International Journal of Engineering Technology, 34 vol. 4, no. 2, pp. 259–276, 2016.

[24] Kularatna, Nihal, and Dias, Dileeka. Essentials of Modern Telecommunications Systems,UK, Artech House, 2004 .

[25] Hassan, Mahbub. Wireless and Mobile Networking, USA , CRC Press, 2022 .

[26] Hwang, Jenq-Neng. Multimedia Networking: From Theory to Practice. N.p., Cambridge University Press2009 ,.

[27] Wu, Jinsong, Sundeep Rangan, and Honggang Zhang, eds. "*Green communications: theoretical fundamentals, algorithms, and applications*", CRC press, 2016.

[28] F. A. Mohammed Bargarai, A. M. Abdulazee, V. M. Tiryaki and D. Q. Zeebaree, "Management of Wireless Communication Systems Using Artificial Intelligence-Based Software Defined Radio", IJIM, Vol. 14 , no. 13, pp. 107-133 , 2020.

[29] Florin Radu, Petru A. Cotfas, Marian Alexandru, Titus C. Bălan, Vlad Popescu and Daniel T. Cotfas," Signals Intelligence System with Software-Defined Radio", Applied Sciences, vol.13, no. 8, 2023.

[30] Ali A. Radhia , Hanan A. R. Akkara* and Hikmat N. Abdullah, "SDR-based Intelligent Cooperative Spectrum Sensing for Cognitive Radio Systems", Engineering and Technology Journal, vol. 41, no. 2, pp. 435-445,

Sadeem W. Al-saegh was born in Mosul, Iraq. he obtained his BSc in communication engineering in 2022 he got the first prizes in Huawei ICT competition national final 2022 and the second prize , second and second prizes in Huawei ICT competition ME&CA and the second prize in prizes in Huawei ICT competition global final , and got the HCIA. he Interested and have high knowledge and experience in subjects of programming ,DSP, digital communication, networking, microcontrollers and ICT.

Dr. **Mohamad A. Ahmed** is an Assistant Professor in Digital Communications. He Received his BSc in Electrical Engineering (Electronic and Communication) from Mosul University, Mosul, Iraq,in1999. He received his MSc with distinction and PhD in Communication and Signal Processing at the School of Electrical and Electronics Engineer ing, Newcastle University, Newcastle Upon Tyne, UK. in 2009 and 2017, respectively. His research emphasized on the field of signal processing for wireless communications. He is also an associate fellow of the UK Higher Education Academy (AFHEA).

Dr. Mahmoud A. Al Zubaidy was born in Mosul, Iraq in 1967. he obtained his BSc in electrical engineering in 1989, MSc in electronic and communication Engineering in 1995 at university of Mosul, and PhD in communication engineering in 2006. He is interested in subjects of radar signal processing, digital communications, telephony and mobile system.

Abdullah B. Al-Qazzaz born in Mosul, Iraq. he obtained his BSc in communication engineering in 2022 and he is working in an ISP company he is interested in electronic circuit design and psychology.

.