



# Introduction to Special Issue: Design and Performance of Networks on Chip

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**Preamble:** This special issue of International Journal of Computing and Digital Systems (IJCDs) focuses on Design and Performance of Networks on Chip, and publishes selected papers from the 2nd International Workshop on Design and Performance of Networks on Chip (DPNoC 2015), which has been held on August 17-20, 2015, Belfort, France [1, 2], and was organized in conjunction with the 10th International Conference on Future Networks and Communications (FNC 2015) [3]. This workshop represented an international forum for researchers from both academia and industry to expose the latest trends, research findings, and emerging issues in the on-chip networking area and its design and performance. The first International Workshop on the Design and Performance of Networks on Chip (DPNoC 2014) was held on August 17-20, 2014, Niagara Falls, Ontario, Canada [4, 5]. The international workshop DPNoC'2014 was organized in conjunction with the 9th International Conference on Future Networks and Communications, Niagara Falls, Ontario, Canada, August 17-20, 2014 [6].

The DPNoC 2015 workshop has attracted papers from authors from several countries across the world. Each paper was reviewed by the members of program committee. The accepted papers cover a range of topics related to the theme of DPNoC 2015. From the conference accepted papers, only five have been selected to be submitted as extended versions in the special issue on Design and Performance of Networks on Chip in the journal special issue, in addition to one more paper selected from normal submission to the IJCDs journal.

**Keywords:** Networks on Chip, NoC paradigm, on-Chip Systems, VLSI, FPGA

## 1. INTRODUCTION

During the past few decades, technology enabled the aggressive scaling and continuous shrinkage of transistors dimension on modern microchips. This made the integration of billions of transistors on a single chip achievable. With such high integration level available, the development of many cores on a single die has become possible. As the number of cores keeps increasing, the employment of efficient and scalable interconnect fabrics has become imperative. Traditional on-chip interconnect schemes, such as point-to-point, shared bus, and the crossbar, are no longer reliable to provide the necessary communication among the processor cores. Network-on-Chip (NoC) is recently viewed as the ultimate solution for the design of modular and scalable communication fabrics, able to provide support to the integration of complex heterogeneous cores through the standardization of the network boundary. This Special Issue focuses on issues related to architectures and design methodologies of on-chip interconnection networks based on the NoC paradigm.

In this special issue, we present five papers that embody the wide range of issues, approaches and interests in the area of on-chip interconnect networks. The first paper is on "NoC Dimensioning from mathematical models" with authors Virginie Fresse, Catherine Combes, Matthieu Payet and Frédéric Rousseau. They propose a mathematical framework that models the relationship between an application task graph, the communication architecture and the resource usage on platform (FPGA in this case) [7]. The next paper, "The Performance of NoCs for Very Large Manycore Systems under Locality-based Traffic," by Sharifa Al Khanjari and Wim Vanderbauwhede studies latency and throughput of NoCs based on well-known topologies under assumptions of physical data expected in 2023 and

underscores the importance of communication locality [8]. The third paper is entitled “Group based Shortest Path Routing Algorithm for Hierarchical Cross Connected Recursive Networks (HCCR)” and is authored by Omair Inam, Sharifa Al Khanjari, Wim Vanderbauwhede and proposes the Hierarchical Cross Connected Recursive network. The paper develops topological properties of the network and studies its performance for Group-Based shortest path routing [9]. The fourth paper by Michael O. Agyeman, Kenneth Tong and Terrence Mak is entitled “An Improved Wireless Communication Fabric for Performance Aware Network-on-Chip Architectures.” It studies device-level changes to improve the performance of wireless NoCs [10]. The final paper by Jawwad Latif, Sadia Azam, Hassan N. Chaudhry and Tahir Muhammad is entitled “Performance Evaluation of Modern Network-on-Chip Router Architectures.” This paper explores the application of switch folding to Dual Xbar routers, showing tradeoffs between buffer energy and performance [11]. The final paper, “Embedded Systems Design Using Event-B Theories,” is authored by Abdelhamid Hariche, Mostafa Belarbi and Abdallah Chouarfia. It studies a framework for modeling aspects of embedded systems, including NoCs, managing design complexity through abstraction and refinement.

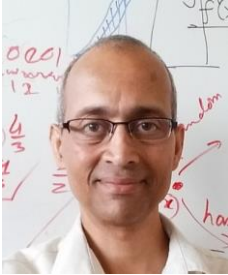
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