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On the Impact of Subnet Clustering in Radio Hub for 100-core Wireless Network-on-Chip Architecture

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Abstract: The integration of numerous embedded cores onto a single die is made possible by the Network-on-chip (NoC), which serves as a crucial technology. The utilization of planar metal interconnects for implementing a NoC through existing methods is inadequate because of the use of multihop channels in data exchange leads to significant power consumption and increased latency. Scalability challenges are anticipated to affect communication systems within many-core architectures expected in the future. As a solution, the Wireless Network-on-Chip or WiNoC design paradigm has been proposed to address these issues. In this paper, we evaluate how subnet clustering in the radio hub affects the 100-core Wireless Network-on-Chip architecture. This study investigates the overall delay in data transmission, the throughput of the network and energy usage in the 100-core WiNoC architecture with equipped with four radio hubs by analyzing single, four, and nine-tile radio subnet clustering. The validation of the results involves simulating the 100-core mesh WiNoC architectures being tested using the cycle-accurate Noxim simulator, with both random and transpose synthetic traffic workloads. Based on the simulation results, the architecture with a four-tile radio hub subnet clustering provides the most optimal performance for both random and transpose traffic distributions at PIR 0.013 flit/cycle/tile when compared to the other analyzed subnet clusterings.

Keywords: Mesh-Based, WiNoC, Subnet Clustering, Radio Hub

1. Introduction

In recent decades, on-chip interconnect architectures have emerged as feasible communication alternatives for chip multiprocessors [1]–[3]. The implementation of multiple core architectures with hundreds or more of processing elements on an integrated chip are now achievable because of developments in semiconductor technology. Chip prototypes featuring multiple cores Network-on-Chip (NoC) architectures have been developed and utilized in a variety of projects, including TILERA [2], RAW [4], SCORPIO [5], and Xeon Phi [6].. The wire delay is a significant concern for the on-chip network system, especially in the context of a large-scale on-chip network, as it can significantly impact the overall on-chip network performance.

The application of networking theory in NoC involves the utilization of packet-switching and a configuration of interconnected routers through point-to-point links, forming a specific topology. Typically, as parallel applications scale, the communication-to-computation ratio tends to increase when the computational workload is distributed across a significant number of cores. With the increasing number of cores, the performance advantages offered by the traditional NoC are limited due to the combination of high latency and power dissipation resulting from long-distance multi-hop communication. Additionally, one of the key obstacles posed by the proliferation of processing cores is the average packet traversal, which impacts the time and energy needed for data movement across the chip die. This necessitates the exploration of an innovative alternative architecture capable of providing shorter distances between the larger processing cores.

However, with the continuous advancements in integration levels, these NoC interconnects encounter significant scalability limitations. This has spurred researchers to explore new emerging interconnect technologies, including optical NoC (oNoC) [7]–[10], three-dimensional (3D) NoC [11]–[16], RF-interconnection (RF-I) [17]–[20]), and Wireless NoC (WiNoC) [21]–[25]. Each of these on-chip interconnect alternatives possesses distinct characteristics along with its own set of advantages and disadvantages [22], [26]. Among various alternatives, WiNoC communication has gained significant attention in recent research due to its numerous compelling capabilities [22], [26]. To begin with, this interconnect is compatible with Complementary Metal-Oxide Semiconductor (CMOS)

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technology [27], enabling its utilization for transmitting data across the chip through a one-hop wireless link. This approach offers low energy consumption, while delivering high bandwidth and low latency. Additionally, since wireless transmission does not rely on physical metal wires or waveguides, the WiNoC platform offers architectural flexibility, thereby reducing area overhead and complexity in chip design.

WiNoC is an innovative Network-on-Chip (NoC) architecture that combines both wired and wireless interconnects to mitigate the inherent long latency of wired planar communication. It achieves this by incorporating an efficient long-range wireless channel [22], [27]–[32]. A group of processing cores is integrated with antennas and transceivers capable of modulating and transmitting data packets for on-chip wireless transmission. Using WiNoC, the distant cores can establish communication with each other through a single hop, resulting in low latency. Furthermore, as the source-to-destination distance exceeds a certain threshold, the performance improvement achieved by utilizing the WiNoC wireless channel becomes more significant. This is because the wireless channel consumes less energy in comparison to the multi-hop traditional metal wire approach [33]–[36].

In order to facilitate communication over long distances among computing cores, this method requires the incorporation of one-hop wireless transmission [27]–[32]. The WiNoC infrastructure includes an integrated transceivers that enables the creation of an immediate wireless medium for packet transmission throughout the on-chip interconnects, especially across far distances [30], [37], [38]. The key network characteristics of the WiNoC architecture, including its topological organization, data flow governance, and routing system have a substantial impact on its overall effectiveness as a network system [39]–[43]. Hence, the primary objective of this paper is to evaluate the impact of radio hub subnet clustering on a WiNoC network system comprising 100-core.

Traditionally, chip design engineers have relied on their expertise, intuition, and specific design objectives to choose a routing algorithm. However, this approach is not always effective because it may not yield the expected performance across different network parameters and various applications. Gogoi et al. suggest a new method that is driven by application patterns, involving a dynamic routing strategy tailored for specific applications to optimize performance [44]. They introduced a machine-learning-based predictive model to classify traffic patterns with a high accuracy of 94.78%. This methodology not only improves network performance, including power consumption and throughput but also simplifies the decision-making process for design engineers. By automating the complex and tedious task of routing decisions, chip designers can focus on other crucial aspects of chip design.

NoC architectures are essential due to their complexity and importance, playing a crucial role in the development of multi-core general-purpose processors and application-specific integrated circuits (ASICs) systems-on-chip (SoCs). These foundational architectures provide insights into their significant contributions to the progression of intricate chip designs and enhanced functionalities. NoC aims to achieve high throughput, low latency, and minimal area consumption. However, conventional NoC router microarchitecture faces issues such as critical path delay, circuit complexity, power efficiency, and resource utilization and timing. Reliance on intellectual property also raises safety and security concerns for SoCs. In [45], Parepalli et al. outline various NoC router architectures and explore distinctive parameters of NoC relevant to numerous FPGA families, aiming to address and mitigate the aforementioned challenges.

Yazdanpanah et. al presented a configurable energy management component for low power of transceiver WiNoC design [46]. Their proposed scheme dynamically adjusts voltage levels and manages power source operations in a distributed style. This technique results in reduced latency and improved energy utilization excluding a significant increase in area hardware overhead. In addition, when evaluated with multi and single chip system, this technique provide improved throughput and reliability. Besides, Balakrishnan et al. proposed improving the scalability of mesh topology in Network-on-Chip (NoC) architecture by incorporating a congestion aware router module [47]. They introduced a minimal DOR XY routing scheme that is sensitive to congestion level, efficiently detecting congestion within the router module while keeping hardware requirements to a minimum. The validation results show that this routing approach leads to a notable reduction in packet latency, particularly when medium packet injection rates are considered, in comparison to the conventional RCS, XY, and GCA routing techniques.

Kavitha et. al proposed contention free ORNoC, the Optical Ring NoC architecture. Kavitha et al. proposed a contention-free ORNoC, the Optical Ring NoC architecture [48]. For handling simultaneous communication, the automatic communication matrix is adopted to assign a single waveguide/wavelength pair. For handling simultaneous communication, the automatic communication matrix is adopted to assign a single waveguide/wavelength pair. From evaluation result, ORNoC architecture shows and attractive results among all the wavelength routed in the optical chip network. From the evaluation result, the ORNoC architecture shows attractive results among all the wavelengths routed in the optical chip network.

Based on study from Pullaiah et al. propose BA-NIS, the hybrid Base-delta Neighborhood Indexing Sequence compression method that adapts zero- and one-based traversals for incompressible chunks of delta compression

[49]. The proposed algorithm is robust against packet loss and can lead to important power savings. It is also effective at compressing all chucks in the data packets. Further, the proposal of a dynamic header flit extension can provide unlimited scalability. Evaluation results show that the proposed work reduces the hardware overhead while obtaining a mean compression of 0.73 and a 51% reduction in latency when compared to the baseline router without any compression.

Zhou et al. introduces a novel architecture, BandExp, that enables subnets bandwidth expansion by using an idle physical links of different subnets [50]. This increased bandwidth accommodates mitigation of the performance loss and serialization issue. In turn, it allows other subnets to have longer sleep cycles, leading to enhanced energy savings. Evaluations showed that BandExp outperformed the Catnap design architecture, reducing execution time and average packet latency by 3.2% and 19.3% respectively. Furthermore, it lowered the net static energy of the system by 23.2% on average, with only a minimal area overhead of 1.3%. Furthermore, Lyles et al. proposed the packet-switched superconducting temporal NoC, or PasT-NoC, dedicated for a scalable power- and area-efficient superconducting NoC [51]. For area optimization, the BDFC is combined with PaST-NoC. Adopting race logic, the packets encode their destination while carrying a collection of data pulse trains. For long packets, the PaST-NoC provides an attractive performance with as much as 5× the throughput per area as compared with the superconducting binary NoC.

This paper is structured as follows: Section 2 reviews the architecture of the 100-core mesh-based Wireless Network-on-Chip, the design of the radio hub transceiver, and the deterministic XY routing technique. Section 3 describes the experimental configuration for the Noxim cycle-accurate simulation. Simulation results and discussions are analyzed in Section 4. Finally, Section 5 concludes the study and offers recommendations for subsequent work.

2. 100-core Mesh-Based WiNoC

A. *Mesh-Based Network Architecture*

WiNoC is an extension interconnect for NoC, and offers a solution to mitigate the significant transmission latency associated with conventional wired communication by integrating both wired-wireless connections in the establishment of efficient wireless communication communication [22], [27]–[32], [52]. Furthermore, due to the progress in on-chip radio transceiver integration [37], [38], [53] and the compatibility if the CMOS mm-wave antennas [54]–[56], the WiNoC design has emerged as a possible improvement to the conventional NoC system [57].The topological structure used for connecting components in a WiNoC has a critical influence on the architectural cost and system's performance. Therefore, it becomes a crucial aspect to take into account throughput the designing phase. Key factors affecting the design of a WiNoC architecture involve various aspects such as the interconnections among processing IP cores [58], [59], encompassing the physical layout, and transceiver design [60]–[62].

Figure 1 illustrates the 10×10 multicore and uniform placement of 2×2 radio hubs across the mesh-based on-chip networks. By integrating radio transceivers into the NoC tiles, it allows for wireless communication between IP processing cores located at considerable distances in proximity from each other directly, leading to single-hop wireless connectivity for WiNoC. Due to the absence of the need for wired path infrastructure between processing cores, the flexible architecture of WiNoC emerges as an appealing choice for future Chip Multiprocessors (CMPs) aiming to address the challenges posed by a substantial number of cores [26], [63]–[65].

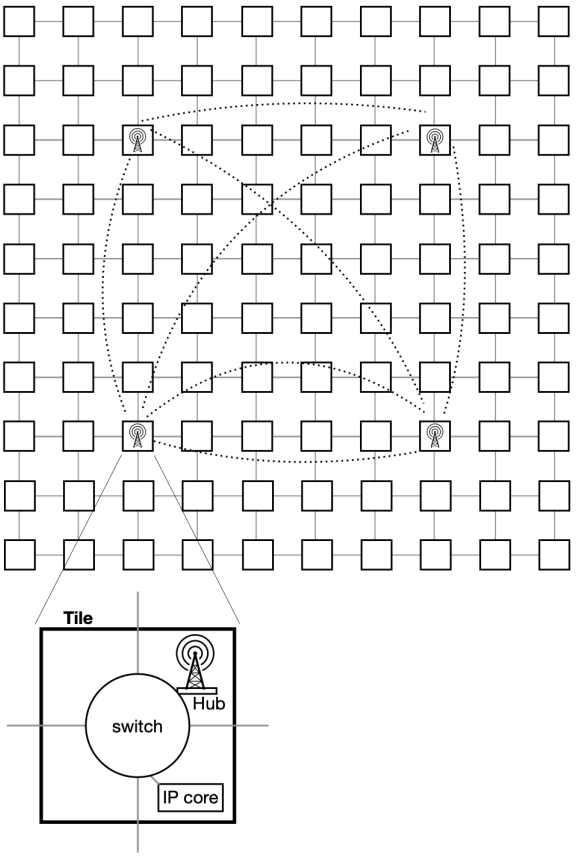


Figure 1. 100-core mesh-based WiNoC architecture equipped with 4 radio hubs.

The majority of WiNoC architectures proposed in the existing literature have embraced regular topological structures to capitalize on their modular, scalable, and straightforward nature [25], [27], [31], [66]–[69]. In these architectures, each radio hub consists of an antenna and a transceiver, forming clusters with a shared wireless

bandwidth among a group of processing cores. The mesh topology is highly appealing for general Chip Multiprocessors (CMPs) due to its distinctive features, including its ease of layout which is well-suited for CMOS silicon implementation, scalability resulting from its regular structure, and the provision of pathway diversity [28], [62], [70], [71].

B. Designing transceivers for millimeter-wave frequencies

Wireless communication systems rely heavily on transceivers operating at mm-wave frequencies, which play a crucial role in enabling high-speed and high-bandwidth data transmission. One crucial aspect that determines the effectiveness of the WiNoC architecture is the design of the radio transceiver. In addition to high bandwidth, the network system that has minimal energy consumption is a desirable requirement for on-chip WiNoC, and this can be achieved through an efficient radio transceiver design. The frequency spectrum of mm-wave, ranging from 30 GHz to 300 GHz, provides a substantial amount of available bandwidth that can be utilized in the WiNoC infrastructure.

Figure 2 illustrates the fundamental elements of the radio transceiver. The transmitting end of the wireless transceiver is composed of up of a serializer, an on-off keying modulator, as well as the power amplifier. On the other hand, a wireless hub transceiver's receiving end is constructed of several components, including the low-noise amplifier (o amplify signals while minimizing unwanted noise), the envelope detector (for detecting and extracting the envelope variations of the input signal), the baseband amplifier, and a demodulator-deserializer for demodulating the received signal and converting it from its serialized format to a more usable form.

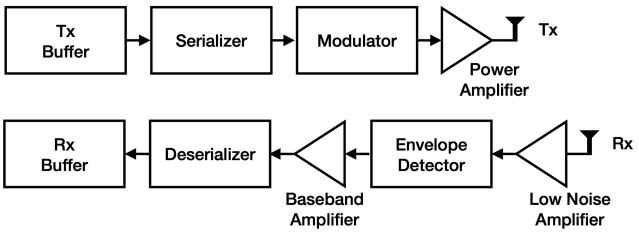


Figure 2. A transceiver utilizing on-off keying (OOK) modulation technique and operating at millimeter-wave frequencies.

C. Deterministic XY Routing Algorithm

Deterministic routing scheme is a favorable routing strategy for typical CMP applications with restricted buffering resources due to their strict latency requirements. Within this wormhole based routing scheme, a packet will be fragmented to flow control digits, also known as flits. All of the routing information required to direct a packet through the WiNoC network is stored in the header of the flit within the packet. If congestion occurs on the network and the header of a flit is obstructed, all of the following flits must remain at their current tile nodes until it clears. As a result, the need for large packet buffers at each intermediate node is eliminated, leaving only a requirement for small buffers.

The mesh-WiNoC topology is well-suited for deterministic routing strategies since they facilitate the creation of the shortest possible path int between transmitting processing elements. Additionally, this routing technique does not require any tables and guarantees deadlock and livelock prevention throughout the chip network. Figure 3 illustrates the potential directions that can be taken in the XY deterministic routings. The continuous lines indicate the permissible turns. In contrast, the dashed lines indicate turns that are not permitted. For example, the XY routing method allowing each packet initially in the X orientation, succeeded by the Y orientation, in order to outreach its intended arrival destination-end.

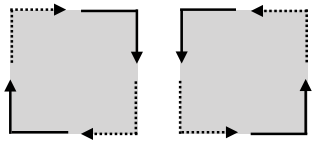
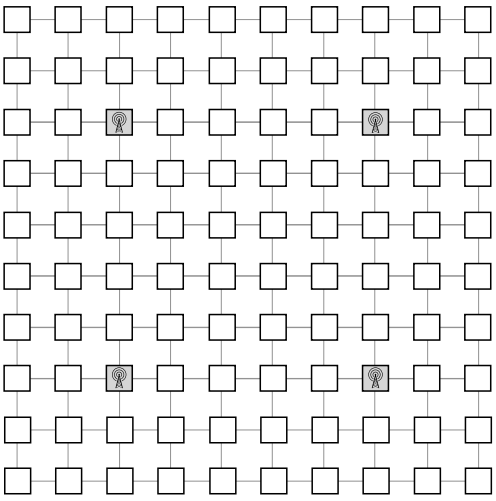


Figure 3. The possible directions for turning in XY deterministic routings.

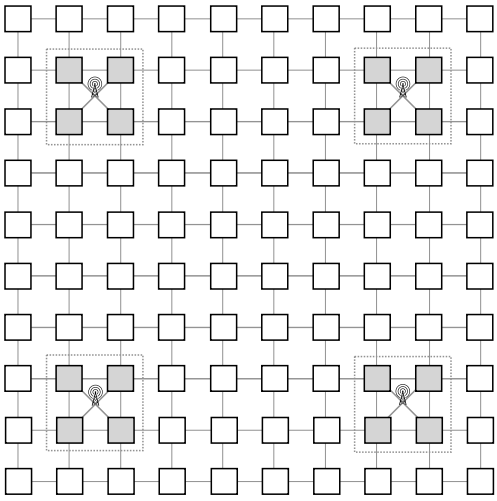
3. Setup for Experimental Simulation

The performance of the examined subnet clustering in radio hub is assessed on the 100-core mesh-based WiNoC topology utilizing Noxim [72], the cycle-accurate on-chip network simulator. The Noxim simulator has the capability to facilitate wireless communication in the mesh-based WiNoC architecture using a wormhole-based deterministic routing technique. In addition, Noxim was also created to enable simple customization for simulating varying designs with distinct traffic patterns. This Noxim simulator precisely models the latency associated with crossbar arbitration and routing path-selection by utilizing real values derived from a prototype router design.

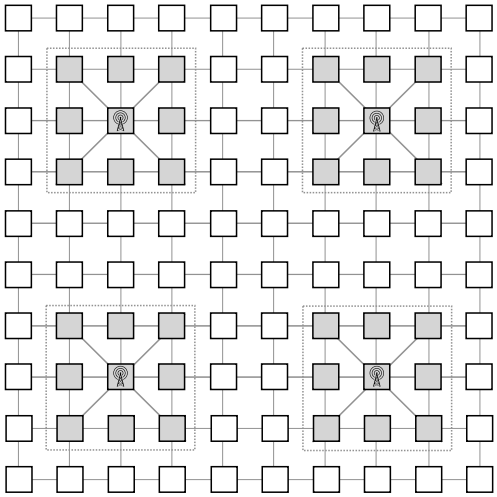
Table I shows the simulation parameters employed in this study. To evaluate the performance trade-off, the simulations were conducted for three distinct subnet clusterings of radio hubs, as demonstrated in Figure 4. Each simulation was executed for a duration of 100,000 cycles. To evaluate the mesh-WiNoC's performance in different traffic scenario, the simulation was carried out using random and transpose traffic distributions. In the case of the random traffic pattern, the processing core has an equivalent probability of dispatching a message to any other tile core. In the case of transpose traffic, each tile located at (x, y), where x and y are between 0 and $E-1$, can only communicate with the processing core located at $(E-1-x, E-1-y)$.



(a) 100-core 4-hub with one tile per-hub



(b) 100-core 4-hub with four tile per-hub



(c) 100-core 4-hub with nine tile per-hub

Figure 4. The architecture of a 100-core mesh-based WiNoC equipped with four radio hub subnet clustering.

TABLE I. Configuration for Noxim Simulation

Parameter	Details
Simulation Time	100, 000 (Cycles)
Total Processing Cores	100-core
Technology	65 nm
Clock Frequency	1 GHz
Number of Radio Hubs	4
Wireless Channel	Single (*mm*-wave)
Wireless Data Rate	16 Gbps
Routing Technique	Deterministic XY
Traffic Distribution	Random, Transpose

4. Result and Analysis

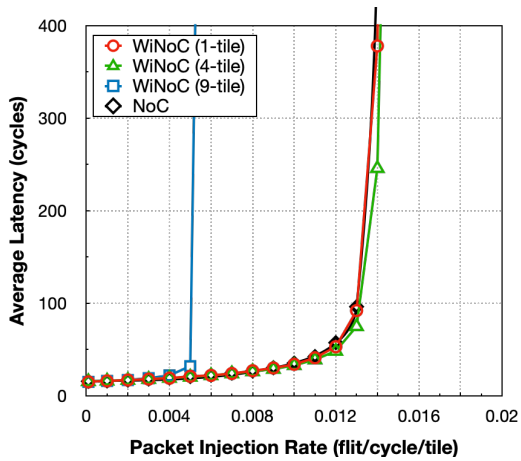
This section discusses the assessment of the 100-core mesh-based WiNoC with subnet clustering in four radio hub performance under two different traffic scenarios: random and transpose workload. The investigated WiNoC radio hub subnet clustering's performance is compared to that of its wired NoC counterpart for the purposes of comparative analysis. The effectiveness of the examined architecture is measured using network throughput and communication latency as performance measures. These measurements are typically used to assess and demonstrate the effectiveness of the WiNoC architecture. Additionally, further analysis is conducted on the energy consumption and wireless usage of distinctive radio hub subnet clusters for both categories of traffic.

A. *Communication Latency Implications*

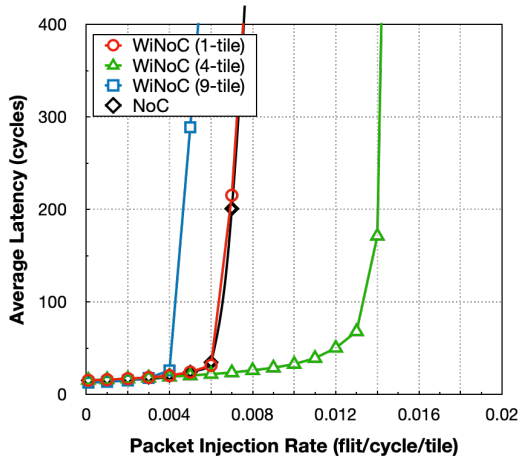
Latency is characterized as the cumulative count of clock cycles required for a data packet from its point of IP core, traverse through the multicore network system, and arrive at its IP destination core's position. The graph depicted in Figure 5 displays the relationship between the injected packet load and the resulting latency. It is evident that the graphs exhibit varying latency values, each with a distinctive curvy shape. With an increase in the packet injection rate (PIR) of the offered load, the latency gradually increases.

Nonetheless, at higher loads, the latency experiences a significant surge with PIR, indicating that the network has reached its saturation point. Meanwhile, Table II summarizes the packet injection rate at the saturation load in flit/cycle/tile obtained in this investigation for the 1-, 4-, and 9-tile radio hub WiNoC subnet clustering, as well as the wired baseline NoC. Meanwhile, Table II summarizes the packet injection rate at the saturation load in flit/cycle/tile obtained in this investigation for the 1-, 4-, and 9-tile radio hub WiNoC subnet clustering, as well as the wired baseline NoC.

In the case of random traffic, the radio hub with single- and four-tile subnet cluster can attain a saturation point of up to 0.013 flit/cycle/tile in terms of packet injection rate. Following that, the nine-tile subnet cluster exhibits saturation loads at 0.005 flit/cycle/tile. In the case of



(a) Random traffic



(b) Transpose traffic

Figure 5. The impact on the network latency for 100-core mesh-based Wireless NoC architecture under various subnet clustering in radio hub.

transpose traffic, radio hub with four-tile subnet clustering can obtain the PIR saturation point of 0.013 flit/cycle/tile.

Subsequently followed by single-tile and nine-tile subnet clustering at 0.006 and 0.004 flit/cycle/tile accordingly in terms of the offered load. Compared to the wired NoC, when subjected to random traffic, the WiNoC with 4-tile subnet clustering exhibits a lower latency of 75 cycles, while the baseline NoC experiences a latency of 96 cycles, despite both operating at a similar saturated load of 0.013 flit/cycle/tile. Furthermore, when considering transpose traffic, the WiNoC architecture with 4-tile subnet clustering demonstrates a higher PIR load of 0.013 flit/cycle/tile, whereas the baseline NoC achieves a PIR load of 0.006 flit/cycle/tile.

TABLE II. Packet injection rate at saturation load under various number of radio hub subnet clustering.

	PIR Saturation (flit/cycle/tile)			
	WiNoC (1-tile)	WiNoC (4-tile)	WiNoC (9-tile)	Wired NoC
Random	0.013	0.013	0.005	0.013
Transpose	0.006	0.013	0.004	0.006

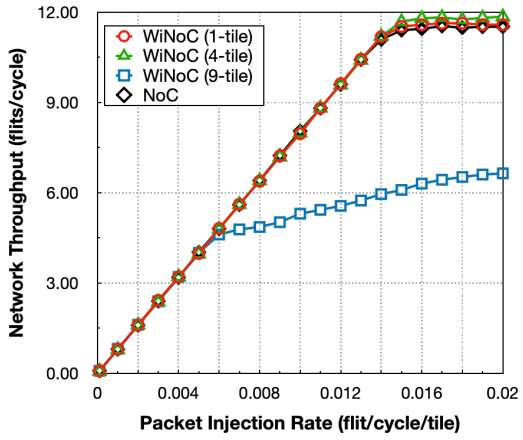
B. Network Throughput Implications

The network throughput can be described as the speed at the transmission of data packets through the WiNoC network architecture. Additionally, the concept of saturation throughput refers to the situation when the network demand reaches its highest point, and the throughput matches the load demand. When the WiNoC network system attains this state, therefore the network becomes ineffective in efficiently transmitting the generated data packets. The 100-core mesh-based WiNoC topology was evaluated by comparing various numbers of radio hub subnet clustering (single-tile, four-tile, and nine-tile) in scenarios involving random or transpose traffic distribution.

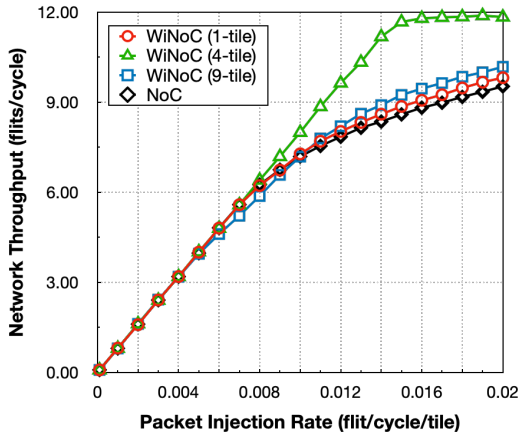
Figure 6 shows the variation in network throughput for incremental PIR workloads. Meanwhile, Table III summarizes the WiNoC throughput at saturation PIR in flits/cycle obtained in this investigation for the 1-, 4-, and 9-tile radio hub WiNoC subnet clustering, as well as the wired baseline NoC. When subjected to random traffic distribution, the saturation points for single-tile, four-tile, and nine-tile radio hub subnet clustering are 4.00, 10.41, and 10.43 flits/cycle, accordingly.

When operating under transpose traffic, the saturation points for single-tile, four-tile, and nine-tile radio hub subnet routing are comparable, with values of 3.21, 4.80, and 10.33 flits/cycle, accordingly. In addition, the network throughput for all radio hub subnet clusters appears to remain fairly steady beyond the saturation point when subjected to transpose traffic, indicating a more consistent network performance.

When examining random traffic, the WiNoC architecture with 4-tile subnet clustering and the wired NoC exhibit nearly identical throughputs of 10.42 and 10.41 flits/cycle, respectively, in comparison to the baseline NoC. However, regarding transpose traffic, the WiNoC architecture with 4-tile radio hub clustering surpasses the wired baseline NoC in terms of network throughput. It achieves a throughput of 10.33 flits/cycle, whereas the wired baseline NoC only manages 4.81 flits/cycle.



(a) Random traffic



(b) Transpose traffic

Figure 6. The impact on throughput for 100-core mesh-based Wireless NoC under various numbers of subnet clustering in radio hub.

TABLE III. Throughput at saturation load under various number of radio hub subnet clustering.

	Network throughput (flits/cycle)			
	WiNoC (1-tile)	WiNoC (4-tile)	WiNoC (9-tile)	Wired NoC
Random	10.43	10.41	4.00	10.42
Transpose	4.80	10.33	3.18	4.81

C. Energy Consumption Implications

In the context of a multicore network system, energy consumption means the quantity of electrical power utilized by the several components and executions within the on-chip WiNoC. Monitoring and managing energy consumption is essential for optimizing network efficiency. The experimental results of the various radio hub subnet clustering for energy consumption, as obtained from the Noxim simulation, are depicted in Figure 7. Meanwhile, Table IV summarizes the WiNoC energy consumption at the saturation load obtained in this investigation for the 1-, 4-, and 9-tile radio hub WiNoC subnet clustering, as well as the wired baseline NoC. The simulations were conducted for both random traffic and transpose workloads. In general, all of the radio hub subnet clustering exhibits an identical energy consumption characteristic. for both investigated traffic. The results indicate that in both traffic scenarios, the radio hub with a single-tile exhibits the least energy usage, with the four-tile and nine-tile radio hub subnets clustering following closely behind in terms of lower energy consumption.

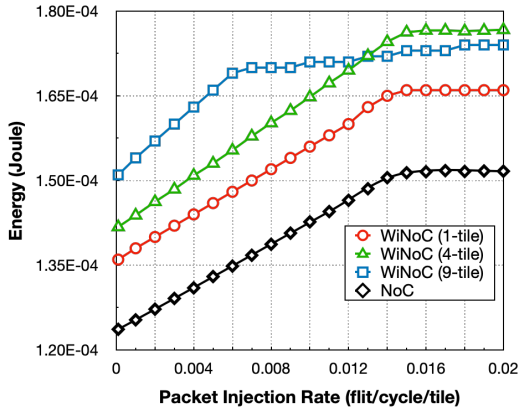
At the point of saturation PIR in the case of random traffic, the energy consumption of a single-tile radio hub and a four-tile subnet cluster are 1.63×10^{-4} J and 1.72×10^{-4}J respectively. For a nine-tile radio hub subnet cluster, the energy consumption is obtained is 1.66×10^{-4} J. In contrast, under transpose traffic conditions, the energy consumption for single-tile, four-tile, and nine-tile radio hub subnet clustering at PIR saturation are achieved as 1.48×10^{-4} J, 1.73×10^{-4} J, and 1.63×10^{-4} J correspondingly. The integration of a radio hub transceiver for wireless communication in the WiNoC architecture leads to higher energy consumption compared to the baseline wired NoC. In both investigated traffic scenarios, the WiNoC with 4-tile radio hub subnet clustering consumes $1.72\times10^{-4}J$ of energy utilization. Moreover, the baseline NoC architecture exhibits energy utilization of $1.49\times10^{-4}J$ and $1.35\times10^{-4}J$ under random and transpose traffic, respectively.

TABLE IV. Energy consumption at saturation load under various number of radio hub subnet clustering.

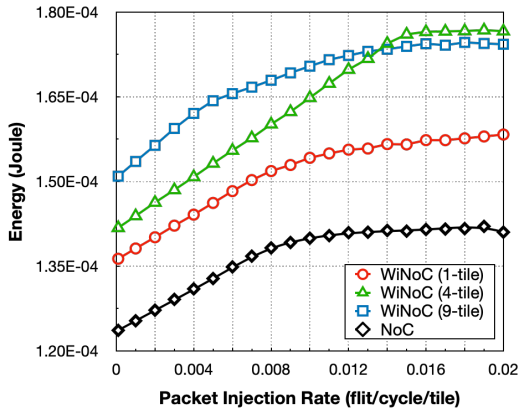
	Energy consumption ($\times10^{-4}$Joule)			
	WiNoC (1-tile)	WiNoC (4-tile)	WiNoC (9-tile)	Wired NoC
Random	1.63	1.72	1.66	1.49
Transpose	1.48	1.72	1.62	1.35

D. Wireless Utilization Implications

The efficiency of wireless resource use in an on-chip network system, including elements like radio hub transceivers, is assessed by wireless utilization. It quantifies the effectiveness of data transmission over wireless mediums. The efficient use of wireless resources is essential for achieving optimal on-chip network performance in WiNoC systems. The proportion of wireless resources being utilized in a WiNoC architecture is expressed as the percentage of wireless utilization. Figure 8 illustrates the percentage of wireless utilization in a 100-core mesh-WiNoC, with varying numbers of radio hub subnet clustering, under both random and transpose traffic scenarios. Meanwhile, Table IV summarizes the percentage of wireless utilization for WiNoC at the saturation load

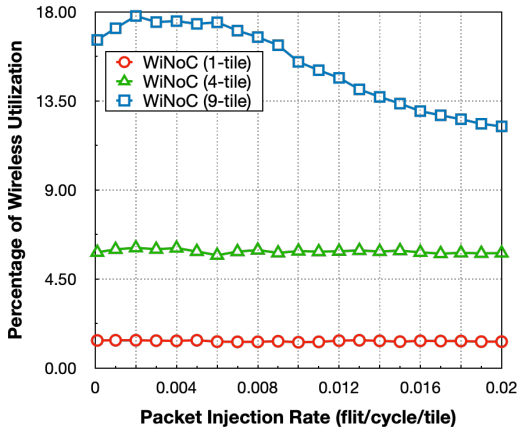


(a) Random traffic

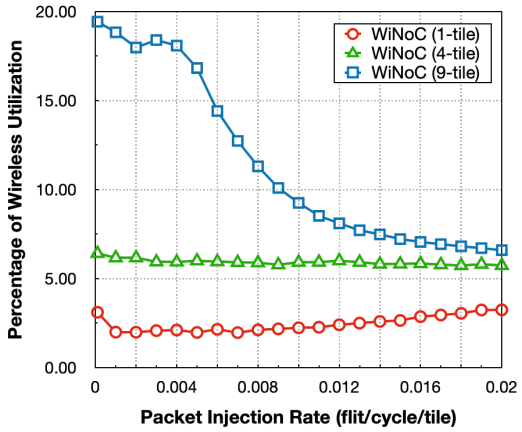


(b) Transpose traffic

Figure 7. The energy consumption of a 100-core mesh-based Wireless NoC with various number of subnet clustering in radio hub.



(a) Random traffic



(b) Transpose traffic

Figure 8. Percentage of wireless utilization for 100-core mesh-based Wireless NoC under various number of subnet clustering in radio hub.

obtained in this investigation for the 1-, 4-, and 9-tile radio hub WiNoC subnet clustering.

Overall, the more radio hub subnet clustering used in the investigated WiNoC system, the higher the percentage of wireless utilization observed. For instance, under random traffic, the WiNoC system's wireless utilization percentage is 1.40%, 5.94%, and 17.39% for single-, four-, and nine-tile clustering, respectively, at the saturated PIR. In contrast, under transpose traffic, the WiNoC system's wireless utilization percentage is 2.15%, 5.92%, and 18.00% for single-, four-, and nine-tile clustering, respectively.

TABLE V. Percentage of wireless utilization at saturation load under various number of radio hub subnet clustering.

	Wireless utilization (%)		
	WiNoC (1-tile)	WiNoC (4-tile)	WiNoC (9-tile)
Random	1.40	5.94	17.39
Transpose	2.15	5.92	18.09

5. Conclusion

The objective of this study was to assess how the 100-core with a four radio hub mesh WiNoC architecture is affected by single-, four-, and nine-tile radio hub subnet clustering. Based on the experimental findings, it has been observed that the architecture with four-tile subnet clustering in the radio hub delivers the best PIR performance for both random and transpose traffic distribution at PIR 0.013 flit/cycle/tile. Under random traffic, the four-tile subnet clustering in the radio hub on the 100-core mesh-based WiNoC network system can achieve a latency of 75 cycles, throughput of 10.41 flits/cycle, 1.72×10^{-4} J energy consumption, and 5.94 % of wireless utilization. Moreover, in the case of transpose traffic, employing four-tile subnet clustering in radio hub on the 100-core mesh-based WiNoC network system can result in a latency of 68 cycles, throughput of 10.33 flits/cycle, energy consumption of 1.72×10^{-4}J, and 5.92% wireless utilization.

In future research, the objective is to explore the impact of multiple channels with adaptive routing on the mesh-based WiNoC network system with a larger quantity of radio hubs, particularly eight and sixteen. Additionally, it would be worthwhile to investigate the WiNoC architecture under assessment with benchmark-specific application workload, such as SPLASH-2 [73] and PARSEC [74], for future research.

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