International Journal of Computing and Digital Systems
ISSN (2210-142X)
Int. J. Com. Dig. Sys. 13, No.1 (Jan-2023)

http://dx.doi.org/10.12785/ijcds/130105

Performance Improvement of Shunt Active Power Filter using Modified Hysteresis Current Controller

Rambir Singh[1], Pradeep Kumar[2], Asheesh K. Singh [3] and A. N. Tiwari[4]

[1]*Electrical Engineering Department, Meerut Institute of Engineering & Technology, Meerut, India*
[2]*Electrical Engineering Department, National Institute of Technology Kurukshetra, Kurukshetra, India*
[3]*Electrical Engineering Department, Motilal Nehru National Institute of Technology Allahabad, Prayagraj, India*
[4]*Electrical Engineering Department, Madan Mohan Malaviya University of Technology, Gorakhpur, India*

Received 7 Sep. 2021, Revised 25 Sep. 2022, Accepted 12 Jan. 2023, Published 31 Jan. 2023

Abstract: Shunt active power filters (APFs) have emerged as a potential player to address power quality issues imposed by exponentially increasing nonlinear loads.The shunt APF used in this work is essentially a three-phase, three-wire PWM based current controlled voltage source inverter (VSI). Hysteresis current controllers (HCCs) are extensively used for gate pulse generation in converter circuits due to easy implementation and better dynamic response. This work explores the possibility of performance enhancement of shunt APF using a proposed modified HCC based on digital logic. The proposed modified HCC based shunt APF provides significant reduction in switching frequency, switching losses, better mitigation of harmonics and smoother reactive power flow. The dynamic analysis of performance of shunt APF with conventional and modified hysteresis current controller (HCC) is performed under randomly varying non-linear loading conditions. The simulated results confirm the ascendency of the modified HCC scheme over conventional HCC under transient as well as steady state conditions. The modified HCC emerges out to be a better scheme with manifold advantages and enhances the performance of shunt APF tremendously.

Keywords: Harmonics Compensation, Hysteresis Current Controller (HCC), Power Quality, Reactive Power, Shunt Active Power Filter

1. INTRODUCTION

The exponential advancement in the field of semiconductor devices and their increased applications has influenced the technological progression in power converter technologies up to a great extent. However, on the other hand, these devices are responsible for harmonic pollution of source current, which may lead to various undesirable events in the distribution system and hence pose serious threat to power quality (PQ). Also, most of the industrial loads are inductive in nature, hence reactive power compensation also needs attention in order to operate near unity power factor. These power quality issues can be very well addressed by using a voltage source inverter (VSI) operating as shunt active power filter (APF) with current control topology, which effectively mitigates the harmonic pollution and reduce the burden of reactive power from the source [1], [2], [3], [4], [5].

The control scheme includes two control loops, one for DC link voltage regulation and the other one to generate switching signals for shunt APF based on the deviation between the reference and actual source currents. The hysteresis current controller (HCC) generate the gates pulses such that the deviation between reference value of current and actual current is minimized and maintained within the hysteresis band.

Hysteresis band of HCC plays a crucial role in governing switching frequency of semiconductor devices. A small hysteresis band ensures that the reference current is impeccably tracked by the source current, to provide better control and effective compensation of harmonic and reactive power. However, a smaller bandwidth of conventional HCC means larger switching frequency. The high switching frequency gives more stress on the devices and results in increased switching losses. Several modifications in HCC have been proposed for different applications [6], [7], [8], [9], [10], [11], [12], [13]. In this work the modified HCC scheme proposed in [7], [8] for controlled PWM rectifier and permanent magnet dc motor drive is extended to analyse the performance of a shunt APF under different non-linear loading conditions. The modified HCC provides reduced switching frequency, less switching losses and also eliminates the requirement of lockout delay between two switches of same leg. The shunt APF with modified HCC provides better harmonic mitigation and smoother reactive power profile as discussed in following sections.

E-mail address: rambir29@gmail.com, pradeepkumar@ieee.org, asheesh@mnnit.ac.in, antiwari2012@gmail.com

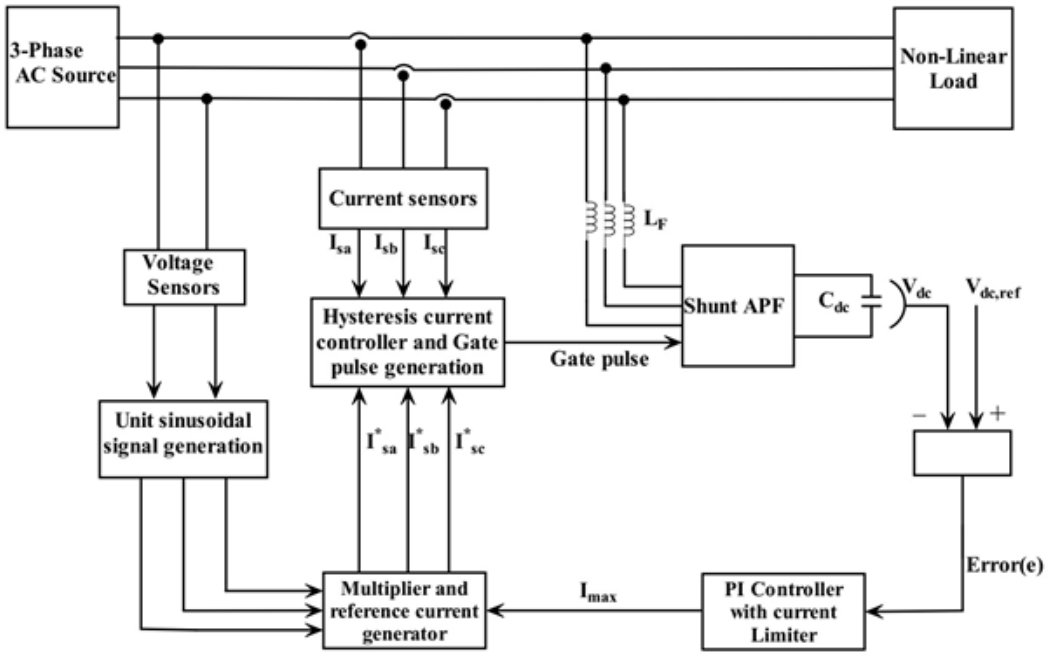


Figure 1. Schematic representation of operation and control scheme of Shunt APF

The remaining sections of the paper are organized in following sequence: principle of shunt APF along with control scheme is presented in Section 2. In Section 3 the conventional and proposed modified HCC schemes are discussed in detail, Section 4 represents simulation results and their analysis, while Section 5 is dedicated to conclusions.

2. OPERATING PRINCIPLE AND CONTROL SCHEME: SHUNT APF

Fig. 1 provides the schematic representation of operating principle and control structure of shunt APF.The shunt APF provides current harmonic compensation by injecting a phase opposite compensating currents, equal in magnitude to the harmonic component produced by the electrically polluted nonlinear load [1], [2], [3], [4], [5], [14], [15], [16], [17], [18], [19], [20], [21]. The phase shifted compensating component cancels out the harmonic current injected due to polluted load, as a result source current becomes purely sinusoidal.

Further, to provide effective reactive power compensation the source voltage and source currents should be maintained in the same phase, irrespective of nature of load. Hence, the phase angle of source voltage is sensed and utilised to generate reference current. The control scheme is implemented to regulate the dc link voltage of shunt APF for effectual harmonic and reactive power compensation. The DC link voltage regulation is accomplished by a PI controller, whose input is the error signal between reference and actual DC link voltages. The output of PI controller is the maximum value of reference source current, which is multiplied with unit sinusoidal template obtained from voltage sensors to generate a sinusoidal reference source current.

In current control loop, the reference source current is compared with its actual counterpart and the error between them is processed through HCCs, to obtain the switching signals for shunt APF. The current control loop ensures that the reference current template is effectively tracked by the actual source current, in order to achieve the desired control objectives.

The reference current template is designed by keeping in mind the basic objectives of compensation principle, i.e., source currents should remain purely sinusoidal and in same phase as that of source voltage.Therefore, it should have a template as given by (1).

$$\left.\begin{aligned} i^*_{sa} &= i_{max} sin(2\pi ft) \\ i^*_{sb} &= i_{max} sin(2\pi ft - 120^o) \\ i^*_{sc} &= i_{max} sin(2\pi ft + 120^o) \end{aligned}\right\} \quad (1)$$

where, i^*_{sa}, i^*_{sb} and i^*_{sc} are instantaneous reference source currents.

3. CONVENTIONAL AND MODIFIED HYSTERESIS CURRENT CONTROLLER

The conventional HCC scheme used for phase 'a' of shunt APF is depicted in Fig. 2. A similar configuration is used for other two phases. The reference and actual source currents are compared, the error signal acts as input for

HCC. The output of HCC is dependent on the value of error signal and hysteresis band. The output of HCC is further used to provide gate pulse to semiconductor switches of respective arm of VSI. To avoid the short-circuiting of dc link during the transition of switching states of the switches on the same leg, a lock out delay larger than the state transition time of respective device is introduced for each switch as shown in Fig. 2.

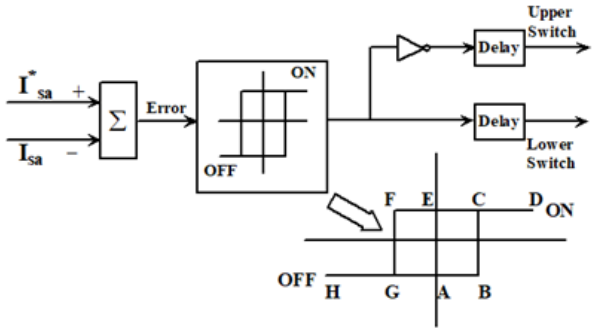


Figure 2. Control scheme using conventional HCC

The switching pattern of phase 'a' of shunt APF is represented by (2)-(3) and summarized in Table I, which covers the entire range of current error.

$$i^*_{sa} - i_{sa} > \frac{HB}{2}, \text{ HCC output = High} \quad (2)$$

$$i^*_{sa} - i_{sa} < \frac{HB}{2}, \text{HCC output = Low} \quad (3)$$

where, 'High' output means switch of lower arm will be 'ON' and that of upper arm will be 'OFF', while it is vice-versa for 'Low' output.Similar switching scheme is used for other two phases.

From Table I, it can be concluded that in mode 2 and mode 6, the state of upper and lower switch changes from their previous state. To avoid the conflict of possible short circuit, requirement of lock out delay is also quite evident. The modified HCC is designed to provide a solution to these conflicts during transition of switching states.

The modified HCC scheme is shown in Fig. 3. In this scheme reference and actual source currents are compared similarly as in conventional HCC.

To implement the scheme two HCCs are required for each phase. One HCC with the same hysteresis band as that of conventional HCC and another is with zero band-width.This modified arrangement provides the solution of the two conflicting transition states of switches in each phase.

The operation of modified HCC for phase 'a' as represented by Fig. 3 is also explained through (4)-(11) under following conditions.

TABLE I. Switching states of phase 'a' devices using conventional HCC

Error					
Made	Sign	Region	Upper Switch	Lower Switch	Conflict
1	(+)	AB	ON	OFF	⊗
2	(+)	CD	OFF	ON	✓
3	(+)	DC	OFF	ON	⊗
4	(+)	CE	OFF	ON	⊗
5	(−)	EF	OFF	ON	⊗
6	(−)	GH	ON	OFF	✓
7	(−)	HG	ON	OFF	⊗
8	(−)	GA	ON	OFF	⊗

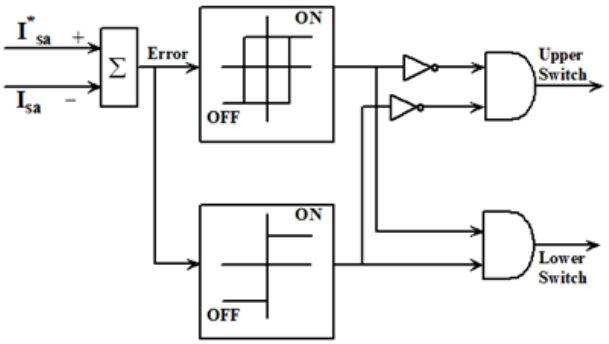


Figure 3. Control scheme using modified HCC

When the error is positive and increasing:

$$i^*_{sa} - i_{sa} < \frac{HB}{2} \begin{cases} \text{Upper HCC output = Low} \\ \text{Lower HCC output = High} \end{cases} \quad (4)$$

$$i^*_{sa} - i_{sa} > \frac{HB}{2} \begin{cases} \text{Upper HCC output = High} \\ \text{Lower HCC output = High} \end{cases} \quad (5)$$

When the error is positive and decreasing:

$$i^*_{sa} - i_{sa} > \frac{HB}{2} \begin{cases} \text{Upper HCC output = High} \\ \text{Lower HCC output = High} \end{cases} \quad (6)$$

$$i^*_{sa} - i_{sa} < \frac{HB}{2} \begin{cases} \text{Upper HCC output = High} \\ \text{Lower HCC output = High} \end{cases} \quad (7)$$

When the error is negative and increasing:

$$i^*_{sa} - i_{sa} < \frac{HB}{2} \begin{cases} \text{Upper HCC output = High} \\ \text{Lower HCC output = Low} \end{cases} \quad (8)$$

$$i^*_{sa} - i_{sa} > \frac{HB}{2} \begin{cases} \text{Upper HCC output} = \text{Low} \\ \text{Lower HCC output} = \text{Low} \end{cases} \quad (9)$$

When the error is negative and decreasing:

$$i^*_{sa} - i_{sa} > \frac{HB}{2} \begin{cases} \text{Upper HCC output} = \text{Low} \\ \text{Lower HCC output} = \text{Low} \end{cases} \quad (10)$$

$$i^*_{sa} - i_{sa} < \frac{HB}{2} \begin{cases} \text{Upper HCC output} = \text{Low} \\ \text{Lower HCC output} = \text{Low} \end{cases} \quad (11)$$

When the error starts increasing from zero towards the positive side but does not exceed the hysteresis band of upper HCC, one of the inputs to both the AND gates is low, so both the devices are in turn off state. As the error crosses the upper hysteresis band both the inputs to AND gate used for lower switch becomes high to turn on the lower device. The upper device remains off. As current error reduces and moves towards zero, the states of devices remain the same unless the current error becomes negative. The moment error crosses zero and enters in negative region, one of the inputs to AND gate of the lower switch becomes low which turn off the lower device with upper device still in off state.

Now the error moves towards lower limit of hysteresis band with both the devices in turn off state. As soon as the error sweeps past the negative lower limit of hysteresis band both the inputs to AND gate used for the upper device becomes high, making the upper device to turn on, with the lower device in off condition. This condition does not change until the current error crosses zero and becomes positive. Table II represents the switching states of phase 'a' devices with modified HCC.

It can be observed from Table II that the devices are turning on when the limits of hysteresis band on either side are exceeded by current error in a way like the conventional HCC. However, the devices are turned off at zero crossing of error and remains off unless the hysteresis bandwidth is not crossed. Therefore, a delay is inherently incorporated between turning on and off of a pair of devices on the same leg. Hence, both the devices remain off before their state transition, to completely avoiding the chance of short circuiting of dc link.

The switching scheme with conventional and modified HCC as applicable to the both the switches of phase 'a' in the entire range of current error is shown in Fig. 4.

As evident from Fig. 4, in case of conventional HCC there is no delay between the state transitions of two devices so the provision of a lock out delay becomes the necessity, which is not the case with modified HCC.

TABLE II. Switching states of phase 'a' devices using Modified HCC

Error					
Made	Sign	Region	Upper Switch	Lower Switch	Conflict
1	(+)	AB	OFF	OFF	⊗
2	(+)	CD	OFF	ON	⊗
3	(+)	DC	OFF	ON	⊗
4	(+)	CE	OFF	ON	⊗
5	(−)	EF	OFF	OFF	⊗
6	(−)	GH	ON	OFF	⊗
7	(−)	HG	ON	OFF	⊗
8	(−)	GA	ON	OFF	⊗

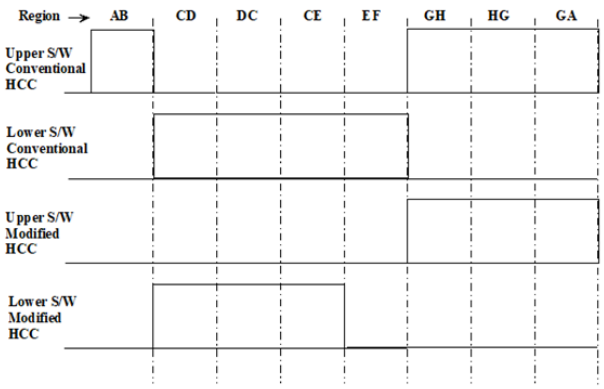


Figure 4. Switching scheme for shunt APF using conventional HCC and modified HCC

4. RESULT AND DISCUSSIONS

A VSI based three phase shunt APF is simulated with both conventional as well modified HCC to evaluate the performance in terms of improvement in THD profile and effective compensation of reactive power with non-linear loading of distribution network. The simulation is executed on MATLAB® Simulink. Selection of system parameters is based on the discussions in [14], [15], [16], [17], [18], [19], [20], [21], [22] and given in Table III.

A rectifier, feeding variable R-L load is used as non-linear load. The nonlinear load pollutes the source current by injecting harmonics and inductive nature of load increases the reactive power requirement. A detailed performance analysis in terms of harmonic mitigation, reactive power management and ripples in reference currents, of conventional and modified HCC based shunt APF is carried out.

The dynamic response of shunt APF is represented in Fig. 5, under variable loading conditions, namely case 1 (switch ON response), case 2 and case 3 (load perturbation, i.e., decrease and increase in load, respectively).

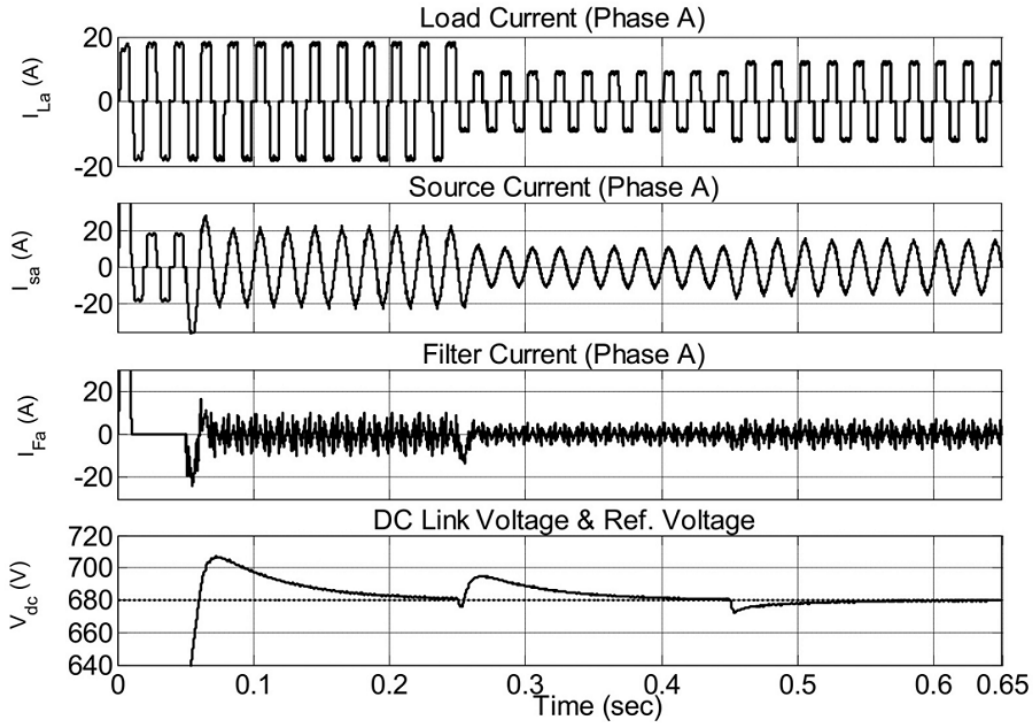


Figure 5. Dynamic response of shunt APF with modified HCC for different loading conditions

TABLE III. Switching states of phase 'a' devices using Modified HCC

Parameter	Value
Supply voltage/phase (V_s)	230 V
Supply frequency (f)	50 Hz
Source side impedance ($R_s + j\omega L_s$)	$(0.1 + j0.157)\Omega$
Interfacing Filter impedance ($R_F + j\omega L_F$)	$(0.4 + j1.051)\Omega$
Reference voltage of DC link ($V_{dc,ref}$)	680 V
Capacitance of DC link (C_{dc})	2000 μF
Rectifier fed variable load resistance (R_L)	$30 - 60 - 45\Omega$
Rectifier fed load inductance (L_L)	20mH

A. *Case 1*

This case analyse the dynamics during switch-on period of shunt APF is represented in Fig. 5. Prior to switching instant, the source current was following the profile of polluted load current with THD of 27.29 %. The moment APF is switched on at 0.05 sec, source current wave shape distortion is significantly reduced, it starts following the sinusoidal profile in phase alignment with the source voltage. The THD settles down under 5% as mandated by IEEE-519 standard [23], just within one cycle of system frequency. The comparative analysis of source current THD with conventional and modified HCC is depicted in Fig. 6(a). The modified HCC delivers better THD mitigation as compared to conventional HCC.

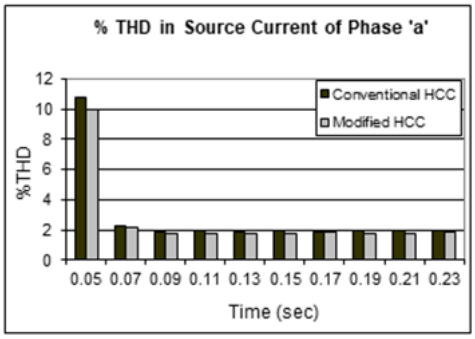
B. *Case 2*

At 0.25 sec, the loading condition is suddenly changed by increasing the load side resistance from 30 Ω to 60 Ω. With increase in load resistance the actual source current reduces and therefore the current error increases and forces the lower device to remain on unless current error reduces to zero. Simultaneously dc link voltage tries to shoot up and is regulated with the help of PI controller by reducing its output. The reduced reference current forces the actual current to follow it. In this case also the harmonic mitigation of source current is better with modified HCC as shown in Fig. 6 (b). The THD even go as low as 1.02% during steady state condition.

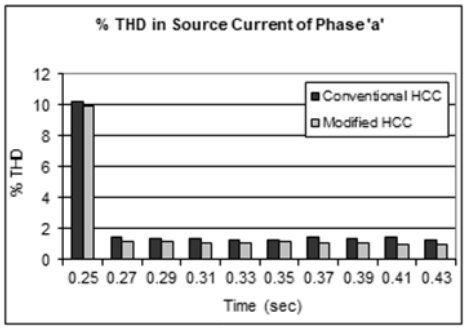
C. *Case 3*

At 0.45 sec, a step change in load profile is initiated from 60 Ω to 45 Ω, the dc link voltage momentarily dips down and then recovers as the voltage error increases making the PI controller to produce increased output. As a result, reference current increases and maintains the power balance. In this case also, the improvement is noticed in source current THD as depicted in Fig. 6(c). The observation of THD profile depicted in different loading scenario of Fig. 6,

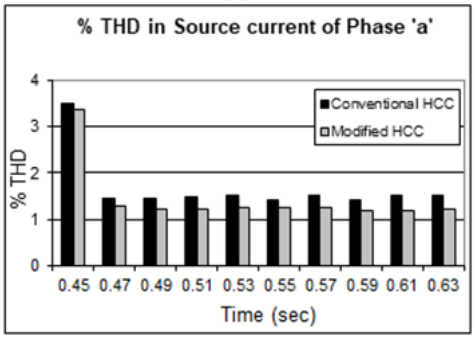
clearly suggest that modified HCC contributes to improve the THD profile of source current. The reduction in THD is caused due to reduced switching cycles and transition of switching states with both switches in off condition.



(a)



(b)

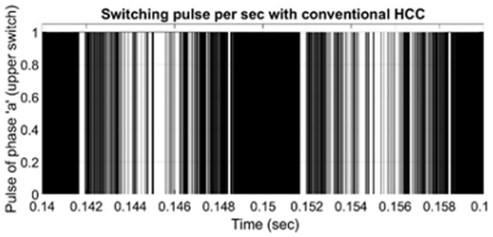


(c)

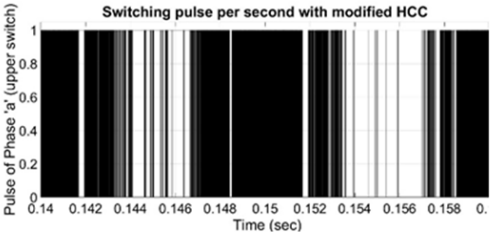
Figure 6. THD profile of source current using conventional and modified HCC with three different load profiles

Fig. 7(a) and (b) represent the switching pattern of upper switch of phase 'a' with conventional and modified HCC. Reduced switching rate can be clearly observed with modified HCC, which in turn will result into reduced switching losses and less stress on the switches. Fig. 8 (a) and (b) demonstrate the effect of HCC on current ripples in reference source current and actual currents with conventional and modified HCC. The ripples in reference source current are more with conventional HCC.

With modified HCC the off period of switches increases, hence current error gets more time to freewheel. In modified

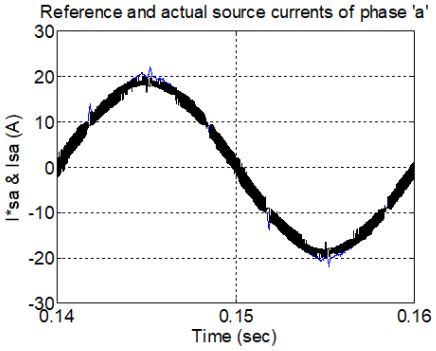


(a)

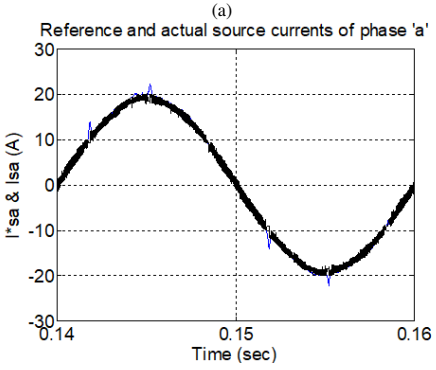


(b)

Figure 7. Switching pattern (a) with conventional HCC (b) with modified HCC



(a)



(b)

Figure 8. Reference and actual source currents of phase 'a' with (a) conventional HCC (b) modified HCC

HCC the freewheeling of current error at zero crossing results in less current error ripples than conventional HCC, where it occurs at upper or lower hysteresis band. This makes the transition much smoother as compared with conventional HCC. Fig. 9 (a) and (b) represent current

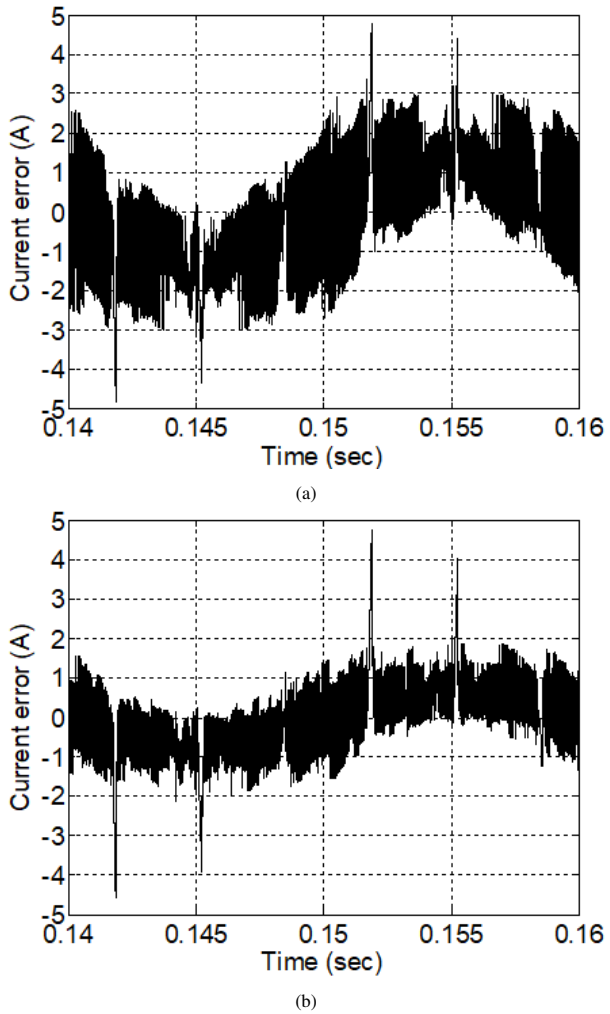


Figure 9. Current errors of phase 'a' with (a) conventional HCC (b) modified HCC

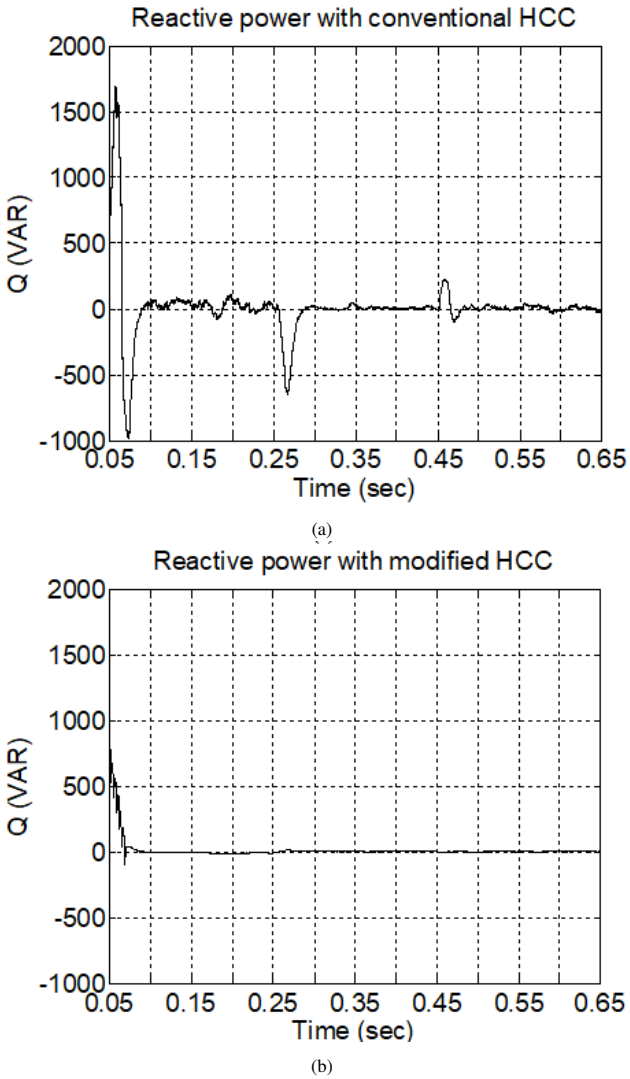


Figure 10. Reactive power compensation by shunt APF with (a) conventional HCC (b) modified HCC

errors of phase 'a' with conventional and modified HCC, respectively. The current error band shrinks in case of a modified HCC. The smaller magnitude of current error in modified HCC establishes the effectiveness of proposed scheme. The reactive power flow from source to load using conventional and modified HCC is presented in Fig. 10 (a) and (b), respectively.

In case of conventional HCC, the reactive power supplied by shunt APF is having large fluctuations throughout the operation. When shunt APF is switched on during the transient period the demand and supply oscillates between 1600 VAR and -1000 VAR as evident from Fig. 10 (a). In case of modified HCC, the reactive power demand is smoothly compensated by shunt APF without any noticeable oscillation as depicted in Fig. 10 (b).

The power balance between demand and supply of reactive power is much smoother in case of modified HCC [24]. Therefore, with modified HCC, there is a considerable improvement in reactive power compensation characteristic of a shunt APF. The ripples and oscillations in reactive power flow have reduced considerably. During load perturbations at 0.25 sec and 0.45 sec, there are noticeable rise and dips in the reactive power flow, in the case of conventional HCC. These transients are significantly suppressed in case of modified HCC and reactive power profile becomes less oscillatory.

A comparative analysis of the performance of Modified and Conventional HCC in terms of peak to peak ripples in actual source current and current errors, along with reactive power management is shown in Table IV. From Table IV, it is evident that modified HCC outperforms its conventional counterpart in reducing the peak to peak ripples and reactive power compensation. The shunt APF with modified HCC

TABLE IV. Comparative Analysis of Peak to Prak Ripples in Source Current and Current Error

Parameter		Conventional HCC	Modified HCC
Peak to peak ripple in source current		3A	2A
Peak to peak ripple in current error		5A	2.5A
Reactive Power during transient condition	Switch ON	1600 VAR/-1000 VAR	750VAR
	change at t = 0.25 s	-650VAR	0 VAR
	load change at t = 0.45 s	250 VAR	0 VAR

does not put any burden of reactive power on the supply side during load change events at t = 0.25 s and 0.45 s. Even during switch ON condition the reactive power compensation with modified hysteresis is much better than the conventional HCC.

The simulation results obtained under randomly varying conditions have confirmed that modified HCC has contributed significantly in the performance enhancement of a shunt APF. The advantages associated with modified HCC are summarised as:

1) reduced switching frequency,
2) low switching losses,
3) inherent lockout delay,
4) due to low switching losses, smaller size heat sinks can be used,
5) smaller magnitude of current error and hence better tracking of reference current,
6) improved harmonic compensation,
7) improved reactive power compensation and smoother reactive power flow.

5. Conclusions

The performance of shunt APF with modified HCC is analysed under randomly varying load conditions. The proposed scheme resulted in fewer ripples in reference and actual source currents, reduced switching frequency and hence reduced switching losses. Due to modified switching, there is no need to have additional lockout delay arrangement between two devices on the same leg which is unavoidable in case of conventional HCC. The freewheeling of current error at zero crossing of hysteresis for comparatively larger time results into reduced current ripples along with smoother switching of devices.

Hence, with modified HCC the shunt APF performs better in terms of improvement in harmonic mitigation, compensation of reactive power, reduction in current error ripples, smoother switching and reduced switching losses. Conclusively, simulation results establish the supremacy of proposed modified HCC over its conventional counterpart in performance enhancement of shunt APF.

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Rambir Singh is associated with Meerut Institute of Engineering & Technology, Meerut, India. His research interests include artificial intelligence, Power quality, smart grid technologies and electric drives.

Pradeep Kumar is associated with Electrical Engineering Department at National Institute of Technology Kurukshetra. His research interest includes computational intelligence and power systems operation.

Asheesh K. Singh is Professor of Electrical Engineering at Motilal Nehru National Institute of Technology Allahabad, Prayagraj, India. His research interests are application of soft computing techniques in power systems, distributed generation, power quality and reliability.

A.N.Tiwari is Professor of Electrical Engineering at Madan Mohan Malaviya University of Technology, Gorakhpur, India. His research interests are electrical power apparatus, power electronics devices, electric vehicles and control of electric drives.