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Degradation of MOS Parameter Due to Bias Instability

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Abstract: Aggressive integrated circuits dimension scaling while the supply voltage is not proportionally scaled leads to reliability degradation. Hot carrier injection (HCI) and negative bias temperature instability (NBTI) effect for Planner MOS Transistor is two primary bottlenecks of the oxide wear-out phase. The lifetime of the devices is truncated by the failure mechanism caused by the aging effect of devices. The accumulation of additional charges into the oxide dielectric and $Si-SiO_2$ interface, resulting in a shift into threshold voltage, mobility degradation, and oxide breakdown, shows prominent degradation into NMOS due to HCI and into PMOS due to (NBTI as a function of electrical stress, stress time, and temperature. The AC voltage stress is lower compared to DC voltage stress, more carriers diffuse to interface at higher voltage, lower thickness, and higher temperature results in a larger shift in the threshold. The lifetime of a device with a continuous supply of higher voltage leads to degradation with the scaling factor. In this work the numerical simulation of HCI and NBTI impact over MOS parameter degradation explored and found that shift caused by NBTI can be annealed with time, HCI cannot be annealed

Keywords: Reliability, Oxide breakdown, NBTI, HCI, Interface Trap, Degradation, Recovery

1. Introduction and Overview

Scaling enables to scale down the dimension of Planner MOS Transistor; excessive scaling of the dimension without proportionally scaling the supply voltage put negative impact over MOS parameter leads to performance degradation. Performance degradation has been listed in the literature of [1] that arose due to the short channel effect which shows a shift in threshold voltage, charge carrier mobility degradation, drain induced barrier lowering, oxide break down. The oxide breakdown leads to permanent damage to the device. The major reasons for the oxide breakdown are exposure to a high electric field with thin oxide layer. The dielectric layer of the MOS device grown by the dry oxidation process must not contain impurity or vacant space. The SiO_2 as the dielectric layer in a MOS device is an important measure to control the channel conduction but opens the door to occurring additional leakage current when oxide breakdown too, which measures the reliability of MOS devices. Electrical defects found near interface of silicon dioxide, while the carrier is flowing through the channel, few of the carrier traps into the interface or penetrated inside the dielectric, depending on the strength of the applied electric field. Scaled devices that possess thin dielectric thickness (t_{ox}) show a significant increase in kinetic energy. These energized carrier strikes with bulk create a free carrier and interface trap into bulk or $Si-SiO_2$ interface discussed in [2]. Created interface trap charge traps can be tuned through the oxide layer provides an additional conduction path from channel to gate terminal through the oxide layer. From the channel, some of the charges are trapped in the oxide layer which results in shift in threshold voltage (V_{TH}). The energized carrier gains significant energy becomes hotter may cross the oxide layer alter the behavior of the oxide layer, multiplies the current. Figure 1 presents the phase of the breakdown model presented in [3] depends on the electrical stress.

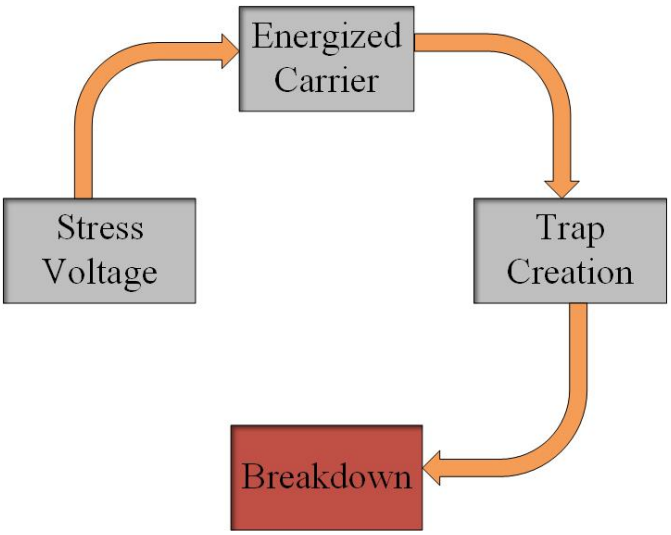

Figure 1. Phases in oxide breakdown [3]

Oxide breakdown is always a serious reliability concern

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in semiconductor devices. Continuous scaling of MOS devices tends to thinner oxide layer (approaches < 50 Å results in higher oxide electric filed at low voltage, low leakage current existsc. The reliability of the dielectric depends on thickness (t_{ox}) of the oxide layer, material defect, and fabrication process. An oxide breakdown instantaneously at 0.08-0.11V per Å. Dielectric breakdown strength is characterized as (a) intrinsic breakdown due to defect generated by electrical stress with usage of the device and (b) extrinsic breakdown due to manufacturing defect. The leakage current gets increases with the application of stress voltage termed as stress-induced leakage current (SILC), lower leakage current in the region of low voltage, due to the electrical stress called wear-out phase. Thin oxide layer with continuous stress sudden jump in gate current seen with noisy known as the soft breakdown, leakage current increase, and follow power-law current-voltage relation. Soft breakdown generally happens due to carrier hopping nearby the trap. With the application of a higher voltage, the carrier in the channel gets energized, penetrates the oxide layer, and creates an interface trap by the charge pump, and leakage current increases. These traps can create a conductive path in the oxide layer. Continuous creation of oxide trap leads to hard breakdown characterize as a large increase in the leakage current.

The lifetime of oxide layer is approximated by the bath-tub curve; failure rate decreasing for the infant phase due to a manufacturing defect. Lower and constant failure rate during useful lifetime and failure rate increases during wear out phase due to aging effect. The occurrence of soft and hard breakdown depends on the breakdown spot and stress condition as shown in figure(2) as a function of applied electrical stress for stress time. Soft breakdown generally occurs in thin oxide, while hard breakdown is associated with the energy discharges through the conductive path form by the oxide trap.

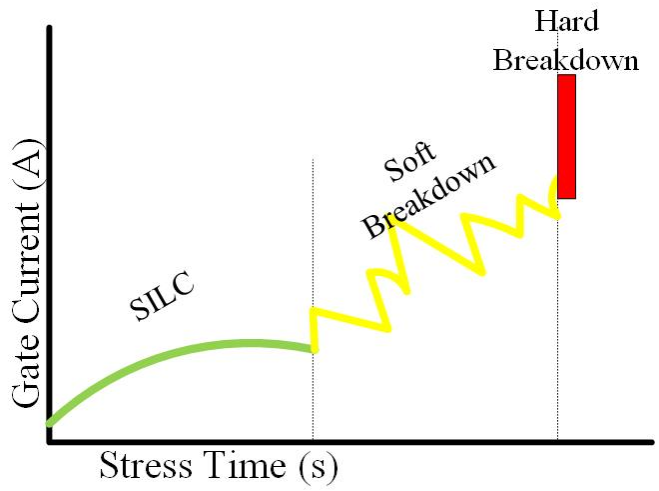

Figure 2. Breakdown with stress time [3]

Reliability measures statically in terms of charge to breakdown (Q_{bd}) and time to breakdown (T_{bd}) described to the Weibull distribution function. The analytical model in [3] can calculate the time to breakdown given as equation (1).

$$T_{bd} = k \times \frac{N_{bd}^{\frac{1}{m}}}{R_G} \times e^{\frac{E_a}{KT}} \quad (1)$$

Where T_{bd} is time to breakdown, N_{bd} is the trap density, R_G rate of generation of oxide trap follows a law of power,$N_{trap}(t) \equiv \alpha t_m$,where m is the nonlinearity coefficient, activation energy E_a and T is the temperature. The remainder of the paper is organized as, 2 elaborates the reason for breakdowns nature, their impact, 3 includes the simulation result, recovery phenomena summarizes in section 4 finally concluded in section 5.

2. REASON FOR OXIDE BREAKDOWN

Oxide breakdown refers to the destruction of the oxide layer of semiconductor devices. The primary reason for degradation is a thin oxide layer scaled less than 3 nm. Carrier in channel under influence of a higher electric field acquires sufficient energy becomes hotter and tunnels between silicon and oxide layer [4] - [5]. Degradation arises due to the formation of the oxide interface trap put the effect on V_{TH} and mobility of the carrier, the variation is time-dependent and degrades the lifetime of devices. Oxide breakdown is classified as intrinsic and extrinsic. Electrical stress-induced defect generation causes intrinsic breakdown whereas extrinsic breakdown due to the manufacturing process. Intrinsic Oxide breakdown is caused due to the bias temperature instability (BTI), carrier injection, and time-dependent breakdown.

A. Bias Temperature Instability (BTI)

Bias temperature instability in MOS i.e., NBTI and PBTI are key reliability issue arises with aging effect result in the shift into threshold voltage and reduction in transconductance. The effect of NBTI is a concern to PMOS because of the negative (-ve) gate to source voltage (V_{GS}). Similarly, PBTI is a concern to NMOS due to the positive (+ve) gate to source voltage (V_{GS}). NBTI is a reliability issue in p-channel MOS devices due to aging [6] due to the capturing of positive charge in oxide and interface trapped reported by Miura and Matukura in [7]. PMOS which operates with -V_{GS}, with continuous usage positive charges are trapped at oxide silicon interface boundary. Eventually, a few of the trap capture in the channel, result in loss of the charge and reduces the drain current. To maintain unaltered drain current higher voltage is needed; threshold voltage needs to increases. The shift in threshold voltage is accelerated by temperature and supply voltage. The trapped charges begin to cancel the carrier contributing to create a conducting channel, these trapped charges dissipate (recovery) over time after removal of V_{GS}. NBTI

has become a critical issue with an introduction to nitrogen along with ultra-thin gate oxide in high-K dielectric and metal gates [8] [9]. The stress and recovery time varies with interface trap density, transistor biasing, and material defect. NBTI induces degradation, approximated as the amount of positive oxide charge and charges in interface states generate, resulting in a shift of threshold voltage to create a conducting channel, the device is considered are failed for a shift in threshold 50 mV or $\delta\ I_{ds}\ /\ I_{ds}\ =\ 10\ \%$ [10]. The shift in V_{TH} approximated as equation (2) [11].

$$\delta V_t(t) = A \cdot t^n \cdot exp(\frac{-E_a}{KT}) \cdot E_{ox}^m \tag{2}$$

Where E_a is the activation energy, E_{ox} electric field across gate oxide during NBTI stress, T is the stress temperature and m, n are model parameters. A larger device puts average behavior and looks identical while scaled devices under a stressed environment the trapped charge spread across and leads to failure. The reliability problem is activated by the degradation of the threshold voltage presented [12]. Figure 3(a) presents the effect of NBTI where the hole carrier is a defect in the oxide layer. These defects can align and can create a path for the carrier in the oxide layer carrier constitute current to flow from gate to substrate. Figure 3(b) the defect formation creates a short between gate to the substrate cannot function as a transistor anymore result in an abrupt gate current indicate failure point shown in figure 3(c). The defect generation process is continuous with time.

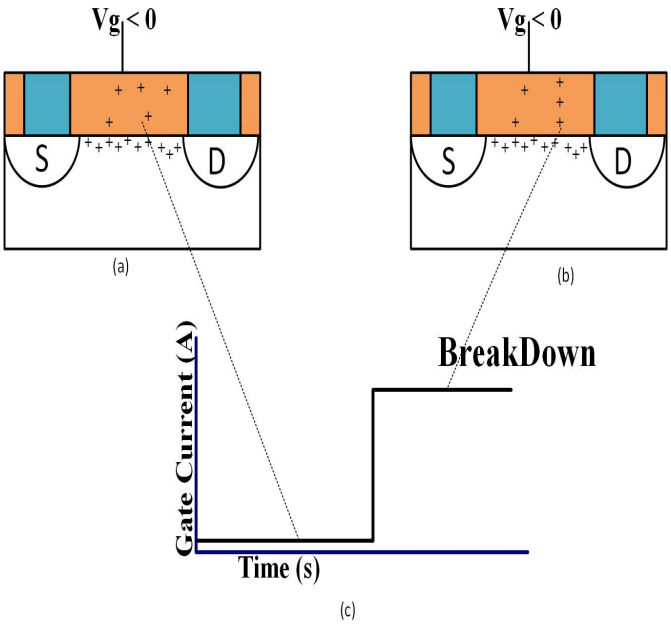

Figure 3. (a)Interface trap creation (b) Alignment of the trap (c) Gate current vs stress time

Modeling of the interface trap generation with the reaction-diffusion model (R-D) presents the depassivation of a hydrogen atom. The V_{th} of PMOS varies with time and different voltage and temperature. When a PMOS device stressed de-passivation of Si-H (dangling bond) in the interface occurs, presented in equation (3) and (4), the hold capture replace the hydrogen atom creates a defect, the hydrogen species diffuses away but device characteristic like V_{TH} mobility drain current degrades with time, the possibility of free hydrogen to react back and remove the interface trap cannot be ignored. The BTI effect on NMOS and PMOS under DC and AC stress follow the $time^n$. The oxide layer grown over pre-silicon through dry or wet oxidation, larger lattice mismatch found between them. Dangling bond due to weak bonds at the interface creates imperfection. NBTI is illustrated in two-phase (a) stress phase V_{GS} applied to the gate charge trap is generated in oxide layer increase threshold voltage and (b) recovery phase trapped charge is release and threshold voltage partially recovered. The transistor enters into the stress and recovery phase alternatively. The percentage of degradation depends on the stress history [13].

$$Si - H \rightarrow Si^+ + H \tag{3}$$

$$Si - H + h \rightarrow Si - H+ \tag{4}$$

The mechanism of NBTI has believed: trapping of charge and generation of interface states are the courses. Into the channel of PMOS have preexisting traps, the dielectric is filled with holes, these traps emptied with the removal of gate voltage, threshold V_{TH} degradation recovers over time. The recovery time is exponential spinning 1us to 10s. A trapped charge may change the dangling bond at the interface. The reaction-diffusion (RD) model describes the breaking of the $Si{-}H$ bond near the Si/SiO_2 interface [14]. In the stress phase (V_{GS} =-V_{DD}) vertical electric file on the gate oxide breaks the $Si - H$ bond, the broken Si bond act as an interface trap while free hydrogen diffused away. In the recovery phase (V_{GS}=0) hydrogen atoms diffused back and anneal to broken $Si - H$ bond, reduce the number of traps and the impact of NBTI disappeared. The number of interface trap densities is approximated as equation (5).

$$\frac{dN_{it}}{dt} = K_F(N_0 - N_{it}) - K_R N_H(0) N_{it} \tag{5}$$

Where N_0 is number of Si-H bond initially N_{it} is the number of interface trap, K_F is the breaking rate under the application of stress and K_R is the recovery rate after removal of stress, H atom defused back. Oxide breakdown is the function of applied electrical stress. The generation of N_{it} during the stress phase results in shift to V_{TH}. The simplified expression under DC and AC stress is given in equation (6) and (7) respectively [15].

$$\alpha\delta|V_{th}(DC)| = K_{DC}t^n \quad (6)$$

$$\alpha\delta|V_{th}(AC)| = \alpha|\delta V_{TH}(DC)| = \alpha K_{DC}t^n \quad (7)$$

Where n is time constant, for Si-H diffusion model n=0.25, t is the time constant and K_{DC} is a proportionally constant. The AC stress is fewer saviors than DC stress, and the perfection parameter α [16].

B. Hot Carrier Injection(HCI)

Hot carrier injection effect in MOS device refers to, a carrier injected from hot conduction channel into the gate oxide dielectric. The requirement from VLSI is to have high-speed devices in a smaller area, scaling features reduce the size in all dimensions makes the oxide thickness much smaller. Short channel devices prefer for higher speed circuit but increase the electric field towards the channel even for lower potential [17]. These increasing electric fields damage the gate oxide interface result in degradation. When the carrier injected in the channel gains kinetic energy becomes hotter (energy requires for electron 3.2 ev and hole 4.6 ev). This additional energy affects the mobility of the charge carrier and path of travel. Hot electrons can tunnel out of the semiconductor instead of conducting through the channel yield a higher leakage current [18] and possibly damage the atomic structure of oxide dielectric. The gain energy of carrier neutralizes in two ways - Carrier strikes the atom of substrate create ion and additional electron-hole pair and carrier randomly strike with Si-H bond breaks create interface trap. This trap leads to threshold voltage shift and degradation of device parameters. HCI arises due to aggressive scaling of device Circuit design without consideration of reliability modeling requires guard band which reduces the performance as well as risk arising with the chip, degrades the device parameter like threshold voltage, transconductance gain, mobility, subthreshold slope due to interface trap created in the gate oxide [19].

Figure (4) presents the occurrence of different failure mechanisms in the CMOS inverter concerning the output signal. It has been reported that the occurrence of HCI on the transition of the device. Bias temperature instability leads to failure in NMOS(PBTI) and PMOS(NBTI) when gate input V_G=V_{DD} and V_G = 0 respectively in the Si to SiO_2 interface [9].

3. RESULT AND ANALYSIS

In this work oxide degradation mechanism due to NBTI and HCI has been explored with an open-source modeling interface generation (MIG) tool available on the Nanohub platform. The MOS parameter degrades more with higher DC and AC stress applied for large stress time and temperature due to build-up positive interface charge.

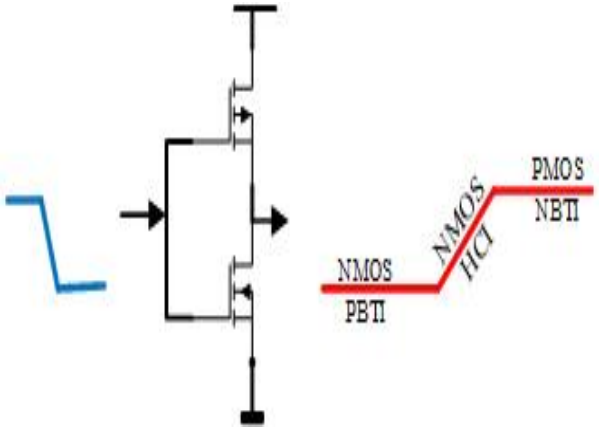

Figure 4. Occurrence of failure concerning the output signal

A. Simulation with modeling interface generation tool (MIG)

The MIG tool models the interface trap generated at the $Si - SiO_2$ interface of PMOS devices [20] - [21]. The tool estimates the variation of the interface trap based on the $R - D$ model discussed in section 2; hence the shift in V_{TH} due to NBTI is based on voltage, temperature, and time [22]. The selected PMOS parameter to investigate the NBTI effect is as follows:- flat band voltage V_{FB} = 1V at which no band bending Effective oxide thickness (EOT) =1.6 nm; scaled physical of dielectric concerning SiO_2 measures as $\varepsilon_{SiO_2} \times \frac{T_{di}}{\varepsilon_{di}}$; Where T_{di} physical thickness of dielectric; ε_{SiO_2} relative primitive of SiO_2 and the relative permitivity of the dielectric layer ε_{di}, whereas substrate doping in N-type substrate is $3 \times e^{17}$ per cm^3 and poly doping is P-type polysilicon doped with $1 \times e^{17}$ per cm^3.

Atomic H and H_2 species are selected for diffusion species and numerically simulated with DC stress 1–3 V and AC stress voltage 1-3 V at frequency 0.001Hz and AC cycle to be simulated 50H. The temperature dependencies of the NBTI follow the Arrhenius diffusion equation of diffusion co-efficient D =D_0 $e^{(\frac{-EA}{KT})}$ where D_0 is diffusion prefactor is $3 \times e^{-8}$ and activation energy $0.5eV$. The dissociation of $Si-H$ bond during NBTI is field dependent and model as Forward Dissociation model [23]. The initial voltage at drain terminal $0.23V$, aging effect diffuse the interface trap requires $0.5eV$ to breaks the $Si-H$ bond. The simulation result shown in figure (5) presents the interface trap generation with a stress time of 10^4 seconds for a maximum lifetime of 5 years. The rate of trap generation with H_2 diffusion species is greater than the atomic H diffusion.

The rate of interface trap generation increases exponentially with higher electrical stress and continuously grows for higher stress times at temperature 70°C. The rate of interface trap generation with H_2 species is greater compare to H species at 1V and 3V, while at 2V opposite relation is found. The lifetime of the carrier in these traps varies

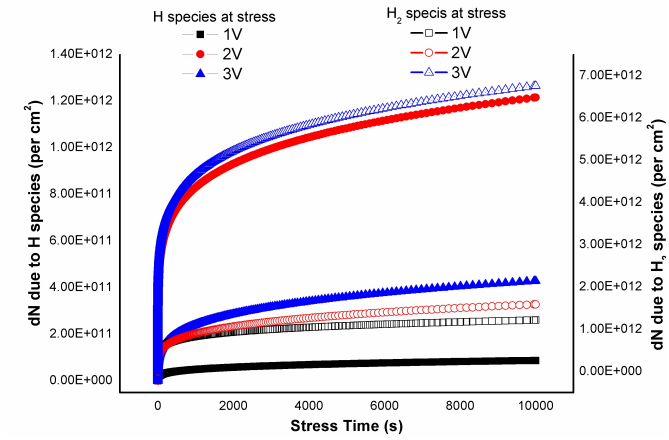

Figure 5. Trap generation vs stress time with DC stress Voltage

with applied electrical stress, few carriers may return to the substrate after a lifetime. Figure (6) presents the projection of carrier lifetime under influence of DC and AC electrical stress. From the simulation result, it is observed that the lifetime of the carrier degrades with a higher supply. It has been mentioned in equation (8) the effect of AC stress is lower than DC stress, interestingly at 1V with DC stress lifetime falls (1.5×10^{8} to 6.5×10^{7}) while AC stress raises (1.5×10^{8} to 2.7×10^{8}) , whereas with higher electrical stress lifetime falls stepper, slope of the falling curve rises with amplitude and frequency.

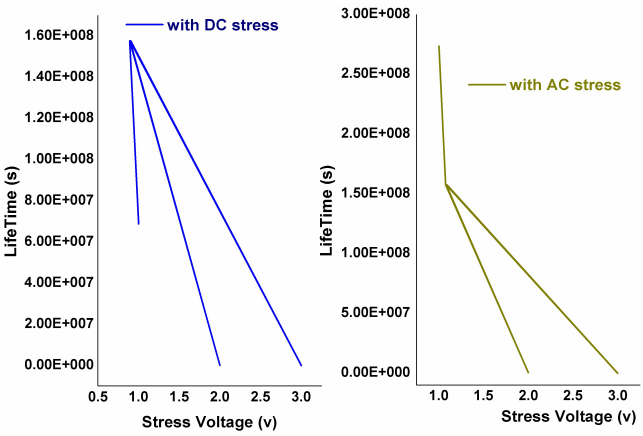

Figure 6. Projection of a lifetime of vs DC and AC stress voltage

One of the most degraded parameters is V_{TH}; presented in figure (7) presents the shift in V_{TH} with exposure of potential 1, 2, and 3V for stress time of 10^4 s. Higher electrical stress generates larger interface density, plenty of carriers in the channel neutralize, result in higher potential at the gate terminal, need to have a sustained inversion channel. At the beginning; stress time 100 s the shift in V_{TH} of is 2 mV and 7.5 mV for stress 1V which rise to 37.5 mv and 117. 9mv for 3V respectively, satisfies the power law of time. The resistance offered by dielectric oxide to free carrier to enters inside oxide differently. A thin oxide layer offers more interface traps compare to thick oxide layers, thus a shift in V_{TH} is lesser for a thick oxide layer. As shown in figure (8) at stress time 100s the shift in V_{TH} is 2 mV and 1.7 mV for 1.6 nm and 3 nm respectively. The shift in V_{TH} reduces with thickness but increases with stress time. Temperature variation is the third parameter that puts additional shifts in the V_{TH}, at the higher temperature, the number of the breaking of Si-H bond enhances the probability of interface trap creation larger at a higher temperature compared to the lower temperature. At stress time 10^4 the shift in V_{TH} are 6.5 mV and 12.3 mV at $70°C$ and $125°C$ respectively presented in figure (9).

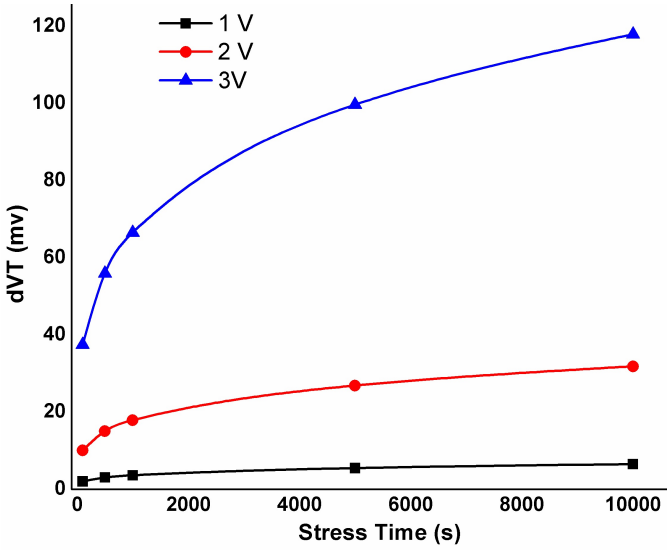

Figure 7. Shift in V_{TH} vs stress time at varied stress voltage

B. *Simulation with Hot Carrier Degradation and Universal Scaling*

HCI degradation is predominantly in NMOS, lower gate voltage field does not attract carrier, if $V_{GS} = V_{DS}$ channel hot carrier injection is maximum, the carrier is attracted by higher electric field across the oxide surface. During stress (high) V_{DS} and (lower) V_{GS} probability of drain avalanche significant, causes by injection of the carrier by avalanche multiplication [17]. The maximum degradation is observed at $V_G = \frac{V_{DD}}{2}$. The R-D model of $NBTI$ modeling not sufficient for HCI modeling since, breaking of the $Si-O$ bond cannot explain universal degradation in hot carrier models the HCI impact.

The degradation modeling tool in Nanobub plots the device degradation at lower bias and high-stress conditions. HCI is significant in NMOS due to the mobility of electrons, HCI occurs when the input to gate transit low to high, shows higher deterioration than NBTI. Unlike NBTI HCI doesn't show recovery. The interface trap is measured through the charge pump current (δI_{CP}), model the universal degradation).Figure (10) presents the universal degradation curve of drain current with drain voltage 5.5 V to 8 V, increase with stressful times. Drain bias 5.5V and 6V curve

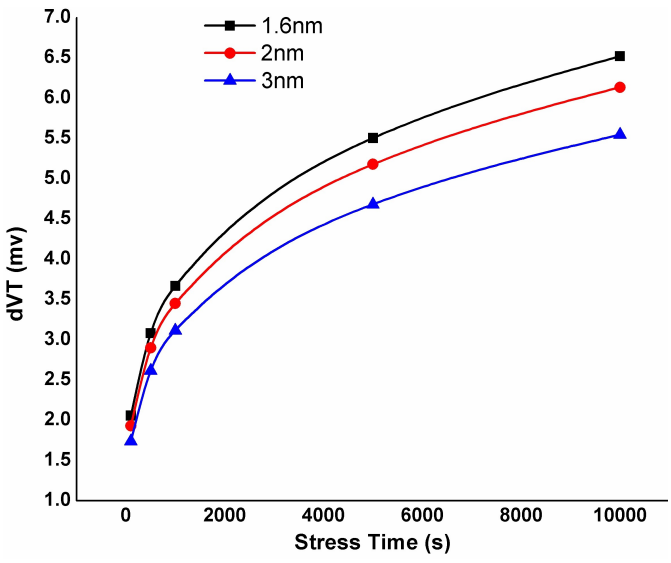

Figure 8. Shift in V_{TH} vs stress time with varied oxide thickness

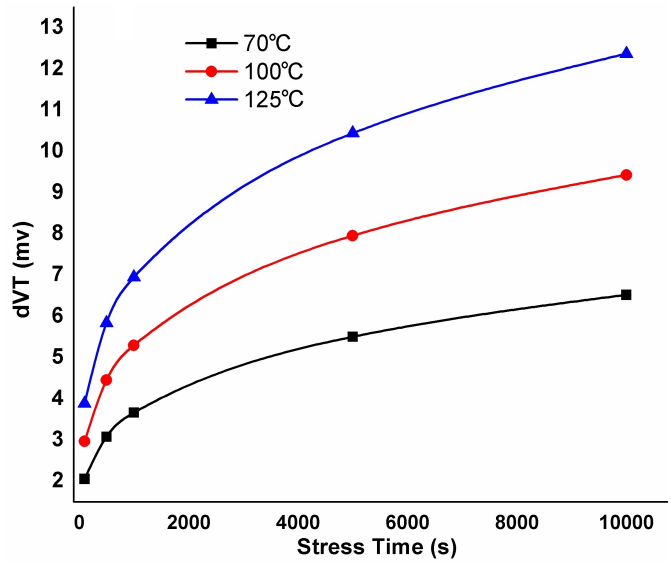

Figure 9. Shift in V_{TH} vs Stress time with the temperature at DC stress 1V

is approximated as linear while for 6.5V to 8V; degradation first reduces than increases because of the initial trap due to acceptor than donors.

$$\delta \times I_{CP}(V_D, t) = f(S(V_D)(t) \tag{8}$$

The changes in drain current due to pumping of charge in the oxide layer given in equation (8) [24] - [25] , where f(S(V_D)) is the universal degradation due to the scaling factor function of stressed drain bias. The scaling factor is proportional to stress drain bias and stress time. Time to reach threshold degradation is known as lifetime measure as the inverse of the scaling factor.

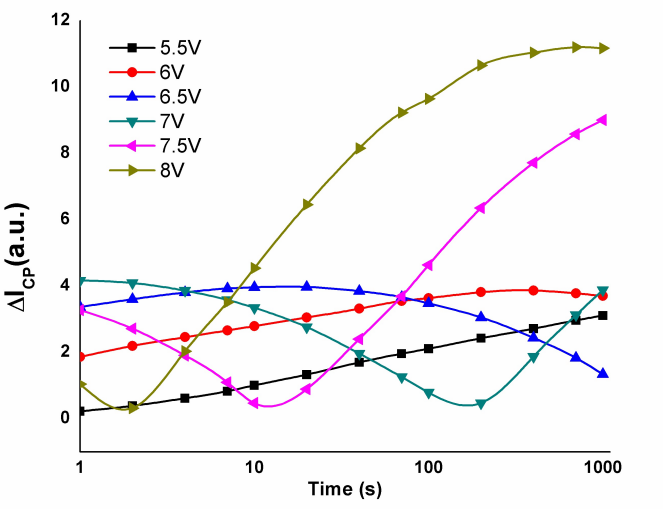

Figure 10. Degradation curve

The scaling factor exhibits the power law of relationship with drain bias given in equation (9). From figure (11) observes that the lifetime of the device is higher for drain bias till 5.5 V and sudden degradation occurs with higher drain voltage. The simulation available to NanoHub Hot Carrier Degradation Universal Scaling explored to perform universal degradation and scaling factor.

$$\frac{1}{S(V_D)} = T_F(V_D) \tag{9}$$

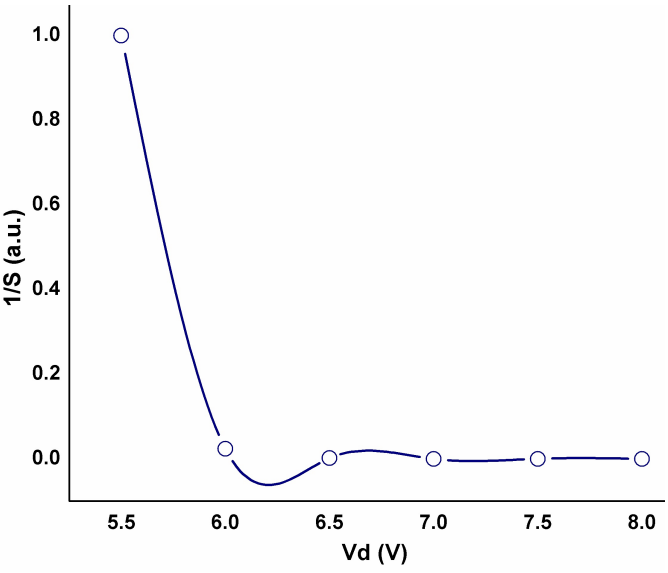

Figure 11. Scaling factor vs drain bias

Degradation in performance parameter due to the cumulative effect of NBTI and HCI; a shift in V_{TH} depends

TABLE I. Shift in V_{TH} due to Oxide Degradation with respect to stress time

Parameter	100 s	10000 s
1 V	2 mV	7.5 mV
2 V	10 mV	31.8 mV
3 V	14.5 mV	94.9 mV
1.6 nm	2.05 mV	6.55 mV
2 nm	1.93 mV	6.13 mV
3 nm	1.73 mV	5.54 mV
343 K	2.05 mV	6.5 mV
373 K	2.96 mV	9.4 mV
399 K	3.88 mV	12.3 mV

on the applied DC stress, oxide thickness, and temperature additionally stress time adds up the square law relation onto degradation. I shows the shift in threshold voltage to NBTI.

4. DEGRADATION AND RECOVERY

Degradation in MOS technology is classified as destructive and non-destructive, HCI and NBTI are Non-destructive while electro-migration, time-dependent dielectric breakdown, broken in physical and electric interconnection is classified as destructive degradation. Non-destructive degradation mechanisms observed in MOSFETs are (a) HCI due to impact ionization of hot carriers to the vicinity of Si to SiO_2 interface, predominantly found in NMOS, and (b) NBTI due to trap generation by cold carrier near Si to SiO_2 interface, predominantly found in PMOS. Energetic hot carriers are the major root cause of HCI degradation which results due to the heating effect of the carrier during normal operation. The hot carrier directed toward oxide surface under influence of electric field involves in breaking of the $Si - O$ bond. The degradation occurs at various levels of electric stress; gate voltage (V_G) $\approx$ drain voltage ($V_D/2$) hot carrier density increase resulting in a significant increase in degradation; for $V_G \geq V_D$ the hot carrier density decreases resulting in a reduction in degradation. Recovery of interface trap is possible during relaxation phase of the PMOS. When $V_G \approx V_D/2$ the HCI degradation is universal and the trap cannot be recovered on the removal of stress. The recovery phase means traps are removed in coexistence between recoverable and permanent damage. There are very few facts known by recovery of the degraded device according to recovery of the HCI degraded NMOS is possible by annealing in nitrogen ambient in the vicinity of interface hydrogen atom interface begin to re-passivates. Since the diffusion rates in Si and SiO_2 are different, the material immediately vicinity of defect matter for recovery.

NBTI degradation is accelerated with electric field and temperature near oxide and recovered as electric field removed. NBTI characteristics are classified as recoverable and permanent. Some part of degradation remain permanent after recovery time and gets accelerated by applied filed and temperature. NBTI degradation and recovery are based on the generation of interface trap, according to $R - D$ model breaking of hydrogen bonds involves at Si and SiO_2 surface. The disassociated hydrogen recombines with a dangling bond and forms Si-H when the electric field is removed.Recovery rate relies upon bias voltage and temperature. Anneal at 350°C to 400°C total recoveries reported in, sufficient hydrogen atoms are present for re-passivation and total recovery takes place. While annealing at a temperature higher than 450°C, provide more thermal energy to break the $Si - H$ bonds defect introduces at the same rate regardless of gate length result in increment into V_{TH}. More trap centers at the interface and diffusion of hydrogen atom take place into the vacuum. In-sufficient hydrogen atom passivation cannot re-accommodate and no significant recovery observed. Gettering of H-atom at the grain boundary not only depends on annealing time but also on cooling rate. A slower cooling rate getter H-atom from a bigger area results in more degradation due to longer diffusion length. Estimation of the degradation important to accurately model the lifetime of the devices. Degradation due to HCI is larger than NBTI and recovery is smaller according to research work in on annealing 1000 s an NBTI stresses device can be recovered can recover 40% while HCI stressed device can recover only 18%. One of the strong reason for it traps generated due to HCI are deeper follows slow recovery rate.

5. Conclusions

In this work, dielectric degradation due to HCI and NBTI has been explored, there root cause and impact of device performance has been simulated with the open-source tool available on the Nanohub platform. NBTI and HCI depend on the breaking of Si-H bonds. Degradation of threshold voltage 117.9V is noted with the electrical stress of 3V. The simulation result of NBTI shows that the impact of DC stress is pronounced compare to AC stress at lower electrical bias. The shift in V_{th} is the cumulative effect of applied electrical stress, stress time, and temperature. Universal degradation model of HCI presents degradation first decreases then increases with stress and time and maximum stress found for gate voltage half of supply. Degradation caused by NBTI can be annealed with time, HCI cannot be annealed.

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