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Static Noise Margin Enhanced in FinFET Based 10T SRAM Cell at 45 nm using EDA Tool

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Abstract: We introduce the parameter that especially affects the stability i.e. Noise. Actually for every Static Random Access Memory (SRAM) cell there is a fix Static Noise Margin (SNM) is present which shows margin of the stability in operations of the SRAM cells. We can analyze the SRAM cells stability and this is done by SNM investigation in read, write and hold mode. In VLSI design, there are many devices facing different-different problems in that concern SRAM cells are defeats the instability of write ability as the technology scaling down destructively. SRAM cells has a dynamic role in a microchip worlds but the scaling down of technology increases the leakage problems more than 40 to 45% than the average power is waste, so due to the leakage and short channel effects. Mostly Complementary Metal Oxide Semiconductors (CMOS) based 7T SRAM Cell has less noise affected due to its one extra transistors controls the output value as compare to 6T SRAM Cells and 10T SRAM Cell. In this paper we work on the FinFET based 10T SRAM Cell that has more controllability over 7T SRAM Cell. So, if we reduce the phenomenon condition of the 10T SRAM Cell that have more FinFET required to build the cell than we can easily reduce the 6T as well as 7T SRAM Cell It reduces the possibility to loss of signals and data. By comparing 7T SRAM Cell and 10T SRAM Cell provides better SNM due to its symmetric & more access controls Cells working. Here, we compare the 7T and 10T SRAM Cell because 7T SRAM Cell has very good SNM than all SRAM cells hierarchy.

Keywords:SNM; 7T SRAM Cell; 10T SRAM Cell; Controllability; CMOS; FinFET.

1. INTRODUCTION

In any Integrated Chips (IC's), memory Cells stability and speed value depends on the average value of the Noise voltage is either Integrated or Spot Noise and resultant value depends on Static Noise Margin [1]. Technologies are reaches towards nanometer range and in these complexities increases due to short channel effect; but the design engineers can only change the cell size of transistors but can't able to remove the drawbacks. The cell ratio (CR) and Pull up Ratio (PR) can be controlled by engineers and by varying these parameters [2], we can control the whole circuitry factors and working. In industries, the circuits and electronics machinery are working on 45nm or less than 45nm technology. Now, the industries are focusing on VLSI circuits that are capable to works on low supply voltages. It affects the SRAM cell performance, variation in data and also reduces the SNM range. The new up-coming performance metric per unit power (Koomey's law), one of the major design optimization alternative is FinFETs, as compared to the planar technology, is much better performance at the same power budget. The FinFETs introduces much higher complexities for resistance and parasitic capacitance [3]. FinFET have many boons over bulk the MOSFETs this are: leakage reduction, sub-threshold level better and voltage gain provide good result. This makes them eye-catching for digital circuitry and low frequency applications, in which the power factor is more important from all parameters. But in high-frequency applications, CMOS based MOSFETs are taken crown of advantage over FinFETs because of their fix threshold and higher transconductance. The FinFET diagram is shown in figure 1 Cross sectional view of FinFET. FinFET has two broad divisions in SOI and bulk FinFET. Short channel effect and high doping cons. Found in bulk FinFET compare to SOI FinFET [4]-[5]. So, FinFET on silicon on insulator is preferred over bulk FinFET [6].

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Double gate MOSFET and MuGFET are floating body devices into which charge trapping occurs in body this causes leakage due to radiation. Charge trapping occurs due to 'back channel interface' and 'total dose latch effect' [7]. Trapping in buried oxide potential of body modulates, when depletion between source and body is lower than electrons injected into the body and drain region collect it [8].If electric field is high to cause impact ionization in drain occur and lead to current runaway causing snapback [9].

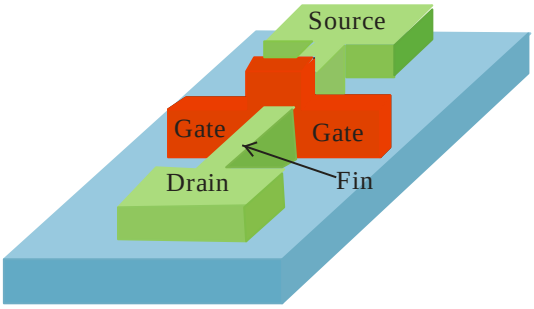

Figure 1. Cross sectional view of FinFET device

For low power application threshold get lowered which also contributes leakage currents.There are many common ways of designing any circuits. One such method is to reduce the power supply around or below threshold voltage [10]-[11]. But lowering the nominal voltage has to sacrifice its functioning to some extent and consequences of lowering the supply voltage are embarrassment in stability of cell, noise margin, on current to off current ratio and strong sensitivity to PVT (process voltage temperature) variations [12]. There are various leakage reduction approaches for both during standby mode and run time that is when the circuit is in operation.The new generation devices we need speed and better storage fast accessing. So, SRAM Cell is fast accessing and storage device [13]. In mobile and RADAR applications, SRAM Cells used with high density on chips, concerns towards excessive power consumption. Scaling down technology affects rise in dissipation of power and other glitches, like noise margin responsibility to get lower for cell firmness arises in bulk 4T and 6T SRAM Cells [14].

For resolving these issues, we analyses the number of FinFET based SRAM Cells topologies that able to operate in a sub threshold voltage successfully. In this paper, we have evaluated the SNM for FinFET based 10T SRAM Cell. Also, we evaluate the SNM curve for write mode because 10T SRAM Cell provide better write ability compare to 7T or 6T SRAM Cells. In many SRAM Cells there is write ability issues affects due to transistors works in sub-threshold region. So, to avoid these issues we switched from 6T, 7T to 10T SRAM Cell.In this paper, we did sectioning of whole paper section 2 gives the brief about working of conventional 10T SRAM Cell then section3 detailed about why FinFET based 10T SRAM Cell and its features. Section 3 contains the transistor width modulation effect and which parameters get affect over SNM and at last section gives the description of SNM.

2. CONVENTIONAL 10T SRAM CELL

10T SRAM Cell is connection of two CMOS inverters cross coupled to each other with two transistors both side to access the data of the bit lines BL and BLB that's why it is known as access transistors which shown in figure 2 Conventional based 10T SRAM Cell as M5, M6, M7 and M8 transistors. Out of M6 & M7 controlled by WWL and M5 & M8 is controlled by WL line. Here, two write lines help to increase the write accessibility and also help to reduce the condition of leakage at the time of rise time, fall time and in hold mode. M9 & M10 transistors provides feedback path for M6 & M7 to avoid the loss of data and also retain the voltage in its current state. For M9 & M10 transistors provided separate ground VGND which can vary from 0 to 0.25 V so that we can reduce the sweeping level [15].In read mode, VGND is moving 1 to 0 V and WL are getting high while WWL remain disabled. The data nodes decoupled due to WWL disabled transistors from bit and bit-bar lines. Due to this separation, the SNM of read and hold mode is same in 10T SRAM Cell [16]. The read mode stability is curiously enhanced in 10T SRAM Cell; because hold mode is much larger than 6T SRAM Cell. Depending on the cell data values Q & QB, one of the bit-lines starts discharging after WL is enabled.

During write mode, WL and WWL are goes 0 to 1 for transferring the write value to cell node from bit-lines. During hold mode WL and WWL values are goes 1 to 0 and access transistors get disabled and the storage node Q & QB stores the previous value of the data on that Cell node.

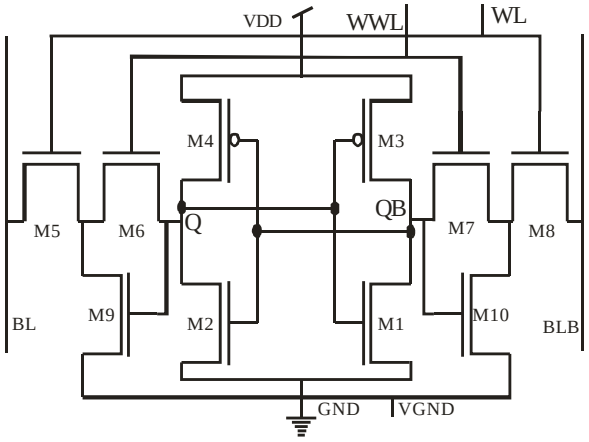

Figure 2. Conventional based 10T SRAM Cell

But, there are some drawbacks in 10T SRAM Cell which reduces the stability of Cell during modes operation to avoid this affects in low power. Either we have to reduce the threshold or we have to leave low voltage working.
Hence, for resolving this issue we switch from CMOS technology to FinFET (Double Gate MOSFET) [17].

3. PROPOSED FINFET BASED 10T SRAM CELL

The working of proposed FinFET based 10T SRAM Cell is same as CMOS based 10T SRAM Cell, into which we just changes the device from single gate to double gate MOSFET as shown in figure 3 FinFET based 10T SRAM Cell. As we know, weak writability is another issue for subthreshold SRAM Cell. In FinFET based 10T SRAM Cell contains series of access transistors in which writability is also a major concern [18]. VDD is getting distorted to enhance the writability due to different-different value which is nearer in low power value. VDD lines are share between the access transistors hence it degrades the hold stability of SRAM Cells. To avoid this issue, each row has to provide separate and individual VDD lines to operate successfully, resulting that cell size increases due to that poly pitch get affected in cell layout. To improve writability we enhance the voltage of WL and WWL by 0.1V in 0.3V VDD to reimburse the weak writability [19]. The schematic diagram of 10T SRAM Cell is shown in figure 3.

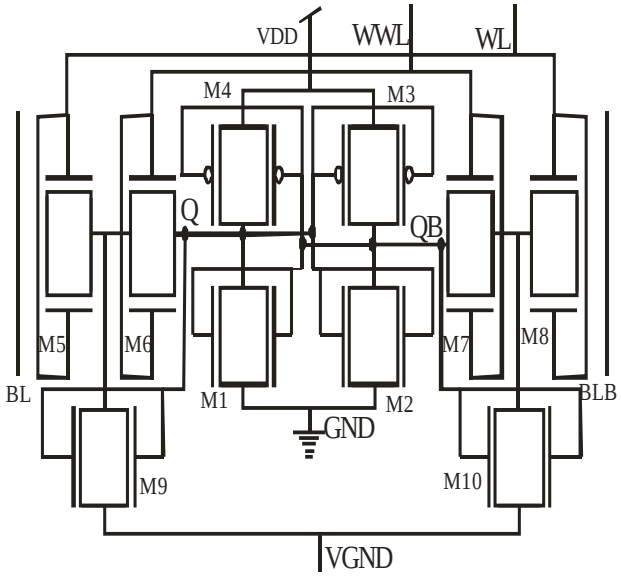

Figure 3. Proposed FinFET based 10T SRAM Cell

4. TRANSISTOR WIDTH MODULATION EFFECTS

The SNM of Read and Write Margin of 10T SRAM cell are affected by the transistor width modulation. The proper sizing of Driver transistor is responsible for a drastic change in the value of SNM. The Cell Ratio and Pull up Ratio affects the stability of the SRAM Cell [20]. The approach that helps to calculate static noise margin is butterfly method. The SNM depends on the following: cell ratio (CR), supply voltage & pull up ratio (PR). 70% stability of SNM is depends on the driver transistors. But, before we can know SNM we have to know the definition of CR and PR. Cell Ratio (CR) is the ratio between sizes of the driver transistor to the load transistor during the read operation.

$$Cell\ Ratio = \frac{Size\ of\ pull\ down\ transistors}{Size\ of\ access\ transistors} \quad (1)$$

Pull up ratio between sizes of the load transistor to the access transistor during write operation. It also fully depends on the size of the transistor [21]. Due to higher speed of evaluation for PMOS transistors in sub-threshold mode, read and write cycle speed are improved.

$$Pull\ up\ Ratio = \frac{Size\ of\ pull\ up\ transistors}{Size\ of\ access\ transistors} \quad (2)$$

5. STATIC NOISE MARGIN

The basic SNM is obtained by mirroring the inverter characteristics and finding the maximum possible square between them. SNM affect both read and write margin that is related to the threshold voltages of the transistors in SRAM Cells [22]. The SNM at 0.7V of 10T SRAM Cell is shown in figure 4 Schematic diagram of 10T SRAM Cell on Static Noise Margin arrangement. The techniques are: 1) increasing the threshold voltage of the access transistors only (M5 & M8 and M6 & M7) changing the word-lines WL & WWL voltage level from VDD in different modes in which we are working at the time of calculation.
A relation of SNM related to transconductance that is:

$$SNM \propto \sqrt{1 - \frac{I_{sd}}{g_{pmos}}} - \frac{I_{sa}}{g_{nmos}} \quad (3)$$

Where the I_{sd} is the saturation drain current of the driver transistor, I_{sa} is the saturation drain current of the access transistor and g is the transconductance.

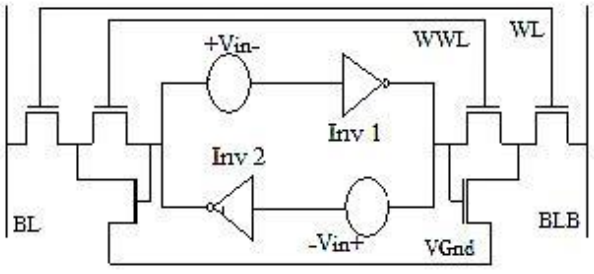

Figure 4. Static Noise Margin establishment in 10T SRAM Schematic during write mode

A. Write Noise Margin and Read Noise Margin

The minimum bl or blb voltage to change the state of SRAM cell from one state to another or from any state to distorted state is write margin. The value of write margin is a function of cell design either symmetric in nature and process variation W/L ratio variation [23].

Write margin is directly proportional to the pull up ratio. In case when we are working on low power supply voltage then it will not help to complete the writing cycle. To discharge storage nodes in write cycle we have to use huge transistors for it. These problems in write margin can be hinder by taking some precautions. Out of this one method in write cycle is to insulate the M3 & M4 from supply voltage. But, this increases the area and reliability also affected.

In 10T SRAM Cell WL and WWL both increases the control over write access but area also increases but it help to isolate the VDD. Based on the transistors current model we can calculate the read noise margin [24]. In calculation of SNM we get the function of the transistor's threshold voltage, power supply and also temperature variation we get the read margin. Read margin is directly proportional to cell ratio. In write mode the stability calculation shown below and its butterfly curve is shown in Figure 5 Static Noise Margin in FinFET based 10T SRAM Cell during write mode.

Calculation for Stability of FinFET based 10T SRAM cell at 100℃

$$NM_H = V_{OH} - V_{IH} \quad (4)$$

$$NM_L = V_{IL} - V_{OL} \quad (5)$$

$$SNM = \sqrt{(NM_H{}^2) + (NM_L{}^2)} \quad (6)$$

Variation of temperature affects the stability as shown in figure 6 Static Noise Margin of FinFET based 10T SRAM Cell with Temperature. As the temperature we vary the butterfly size varies, so the Static Noise Margin also varies. Here, we vary the temperature from 27℃ to 100℃. The variation is shown in Table 1 and comparison of SNM of write mode value is shown in the figure 7 Comparison of FinFET Based 7T and 10T SRAM Cell on various temperature ranges.

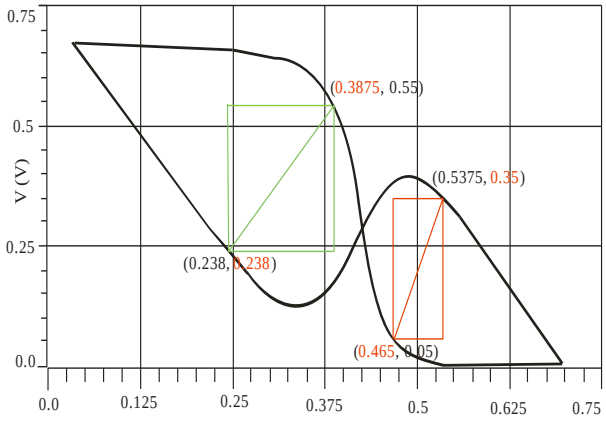

Figure 5. Static Noise Margin in FinFET based 10T SRAM Cell during write mode

TABLE I. Variation of SNM by varying Temperature

FinFET Based SRAM Cell	Temperature (in ℃)			
	27	***50***	***80***	***100***
7T SRAM Cell	143mV	139mV	125.26mV	119mV
10T SRAM Cell	148mV	142mV	138mV	136.19mV

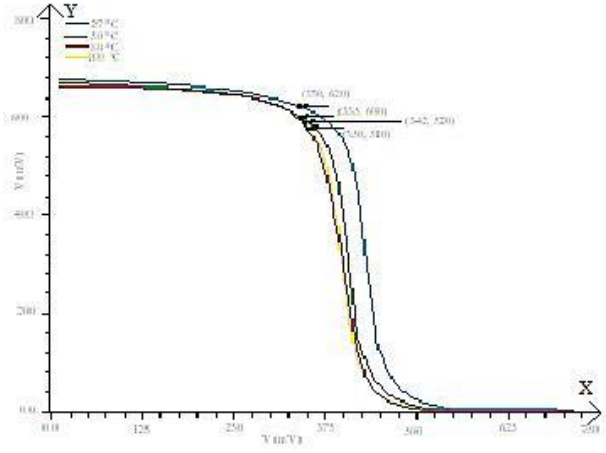

Figure 6. Static Noise Margin of FinFET based 10T SRAM Cell with Temperature

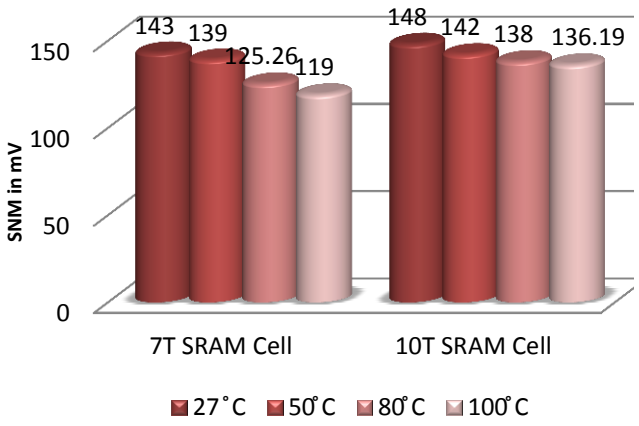

Figure 7. Comparison of FinFET Based 7T and 10T SRAM Cell on various temperature ranges

6. CONCLUSION

In IC designing the major concern we have to take is packaging (density) and lower leakage parameters in that denser medium, but still the reliability issues occurs in the circuitry. When discussing about memories in the IC then that time this issues we have to take seriously out of that Noise is the major issue which affects due to variation of temperature, low supply voltage, and variable threshold voltage. So, to find out the noise margin in SRAM Cell we are applying SNM butterfly curve calculation method on FinFET based 7T and 10T SRAM Cell. Out of that, FinFET based 10T SRAM Cell gives higher and perfect value compare to 7T SRAM Cell. In write mode, the value of SNM in FinFET based 7T SRAM Cell is 119mV but in FinFET based 10T SRAM Cell the SNM value is 148mV. FinFET based 10T SRAM gives improved results in Read SNM and also in Write SNM compare to 7T and 8T SRAM Cell because of its symmetric nature and also its more control over bit lines due to access transistors are double compare to all SRAM Cell. Also, we know that leakage parameters of any circuitry is getting doubled after every 10℃ temperature but the variation in FinFET based 10T SRAM Cell is only varies from 138 to 148 mV but in 7T SRAM Cell its value is varies from 143 to 119mV which shows that the 7T SRAM Cell is less value of SNM value as compare to 10T SRAM Cell.

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