International Journal of Computing and Digital Systems

http://dx.doi.org/10.12785/ijcds/020309

Analysis and Design of E1 over Ethernet Gateway

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Received 30 Jun. 2012, Revised 5 Nov. 2012, Accepted 30 Jan. 2013, Published 1 Sep. 2013

Abstract: The most commonly used technique in networking nowadays is packet switching. It has become one of the important infrastructure elements in the communication society. Time-division multiplexing (TDM) and Synchronous Digital Hierarchy (SDH) over Ethernet is regarded as an economical and efficient scheme in the mid-distance of TDM or (SDH) interconnections. This paper focus on the design and analysis of the E1 to Ethernet protocol converter (Gateway), it based on the frame granularity scheme which takes into account of miniaturization, power, cost and time delay of companding reduction. The E1 to new Ethernet (LAN) link protocol converter designed in this paper utilizes universal programmable devices. A new approach is proposed, modeled and then simulated by using (VHDL) code and implemented in Spartan 3E kit. In high speed networks, packet processing is relatively expensive while bandwidth is cheap. The proposed approach considers the most important factor affecting the performance of high speed networks. These are packet processing time, throughput, and packet efficiency. Packet processing time is an issue in real time communications. As consequences, real time signal quality (like the voice) might be degraded severely when the process time exceed its limits. In this paper, the simulation results show that the active mode of the frame payload effectively improves the performance of the Ethernet protocol. In E1 line, 36% bandwidth is saved at half traffic load of the maximum.

Keywords: TDMoIP, TDMoE, Ethernet, E1, FPGA.

I. INTRODUCTION

At the present time, Ethernet communication products, applications and solution are becoming more entrenched as the most common standard for data transport (carrier). Carriers are reducing costs by eliminating the need for added networks that require different resources for different service types. The primary goal for carriers is to accommodate all of these services on a single network where the Ethernet and IP (Internet Protocol) has this ability clearly [1].

Ethernet technology has evolved to the point, where service providers are beginning to deploy new services to the wide area network. The first task for this technology was to carry a small and slow rate data from the computer to the peripherals at the mid of the seventies from the past century. Soon after that, higher data rate and bigger bulk of data were easily transferred from node to node or to any peripherals like printers, storage devices, etc.

Telephony technology, on the other side, has evolved rapidly where a new generation is shown up every two or three years. Note that compatibility principle enforces the main industrial companies to keep using the old techniques. One of these old techniques is carrying and combines the voice signals in time slots within a frame of at a specific time and speed and then transfer these signal from point (like Private Branch eXchange (PBX)) to another point (like Public Switched Telephone Network (PSTN)). One of the available solutions for the communications service providers and enterprise customers to deploy voice and leased line services over efficient network is Voice over IP (VoIP) which requires an investment in new network infrastructure and customer premises equipment (CPE). The second solution which end user equipment need not be replaced is TDM over Internet protocol TDMoIP, whereby Internet backbone or modern packet switched networks (like 2G systems) can be used for transport. TDMoIP was first developed in 1998 by RAD Data Communications and first deployed in Sweden in 1999 by Utfors [2]. Utfors employed the first generation TDMoIP product (known as Ipmux-4) to provide bundled services including TDM private lines, TDM leased lines and a variety of IP and Ethernet services. In 2001, the IETF set up the PWE3 working group, and which was chartered to develop architecture for edge-to-edge pseudo wires, and to produce specifications for various services, including TDM. Other standardization forums, including the ITU and the MPLS - Frame Relay Alliance, are also active in producing standards and implementation agreements for pseudo wires. Conventional TDM networks are highly deterministic. The circuit delay through a TDM network is predictably low and constant throughout the life of a connection. Conventional TDM networks are highly deterministic with a source device transmitting one or more octets to a destination device. This occurs by a dedicating-bandwidth channel every 125 µs. TDM delivers timing with the data while tightly controlling jitter and wander. Timing is delivered along with the data, and the permitted variability (jitter and wander) of TDM clocks is tightly defined. In addition, the infrastructure supports a rich set of user features via a vast set of signaling protocols [3].

The communication link is providing a constant data stream with a fixed bit rate in TDM network. The higher the bit rate, the higher the bandwidth, and the higher the amount of data that can be transmitted. Ethernet is a technology-based on package. Data is placed to be transmitted to one or more of the packets and then deliver whenever there is available bandwidth, there is a certain randomness introduced. End-to-end delays may not be constant. The data may not even be delivered in the same packet but chopped up in several packets. The receiving application has to put them back into correct order. There are technologies that address these shortcomings and provide solutions for “real time services” such as VoIP (voice over IP) and TDMoIP (Time Division Multiplexing over IP). Another advantage with Ethernet is the plug-and-play nature of network. A TDM network needs to have carefully designed channel allocation to optimize the bandwidth usage. Ethernet is largely self configured in this respect [4].

In this paper the VHDL code used for simulation of the E1 to Ethernet converter in new manner is proposed. This paper is organized as follows: the next Section provides a brief overview of related work in the research area. Section 3 describes TDMoIP architectures and standards. Section 4 describes TDMoE. Section 5 devoted to the analysis of the parameters effect. The proposed gateway is explained in Sections 6. Section 7 describes compression operation. Section 8 explains model analysis. The experimental results are described in Section 9. Finally, conclusions are made in Section 10.

II. Related Work

The TDM data travels through the Internet; an overhead with control information is added to the TDM data payload. The header size is 40 bytes: RTP header; UDP header; and IP header which consume big part of bandwidth. To save the bandwidth, it is Possible to remove these headers and to use the active mode that compresses the TDM data payload without any effect on the communication quality. A number of studies investigated several factors as means for real-time protocol implementation;

Yamamoto [5] provided an experimental study of the effect of packet-size on speech quality. Based on subjective experiments, the authors proposed several equations to describe the effects of packet size variation and packet loss.

Oouchi et al. [6] evaluated suitable voice-packet length in IP packets for the adjustment of VoIP network systems. The researchers used a simple test network and evaluated the effect of changing a voice data length on a packet loss rate. Based on his results, the authors concluded that in most cases, a variable voice packet-length VoIP system would be useful to achieve both high-transmission effectiveness and stable voice quality.

Ngamwongwattana [7], on the other hand, investigated the effect of packet size variation on the end-to-end delay. Due to theoretical studies and simulation he concluded that small voice packet-size is preferred for minimal incurred delay but, because of a large IP-rate requirement, it has the potential to cause congestion, which could result in increasing end-to-end delay. Large voice packet size incurs additional delay due to packetization.

Eugene S. Myakotnykh, Richard A. Thompson [8] investigated the effect of voice payload size and compression variation on VoIP quality under various network conditions.

Barani Subbiah[9] described a new method to multiplex a number of low bit rate audio streams into a single RTP stream between IP telephony gateways. In this paper, they described a new method to multiplex a number of low bit rate audio streams into a single RTP stream between IP telephony gateways.

Junius Kim[10] explained the emulated services, such as CES, allows TDM circuits to be bridged between locations by providing a pseudo wire tunnel across a provider’s IP packet switched network.

This allows the legacy TDM companies to maintain its existing TDM equipments and technology while using advantage of next generation core transport networks, thus extending the life of legacy TDM companies with equipments.

III. Overview of TDM over Packet Switching Architectures and Standards

There are two main architectures for TDM over packet switching, structured and unstructured TDMoIP [11].

A. Structured mode refers to transport of the active TDM channels individually or in groups depending on their destination. Dealing with TDM channels allows individual channel management priority, and quality of service requirements trade-off with a very large number of small packages. TDM channels are collected and sent to the same destination, TDM over packet switching can reduce overhead packets regardless of their priorities.

The disadvantage of this approach is generates more traffic with high priority.

B. Unstructured mode refers to transport of the TDM stream after transparently encapsulated from point-to-point connections over IP network as tube without an understanding of the signaling and TDM services. Silent-suppression can be supported to provide a better utilization of network resources, but with uncontrollable delay since the TDM signal must be packaged and de-packetized every TDM over packet switching network hop.

Congestion in the packet switching network will focus on all strains, which degraded service quality for all calls, including calls with high priority [11]. Many packet technologies will soon displace TDM infrastructure. Fig. 1 outlines the packet format for all of the standards that always include network layer headers and the adaptation layer [1]. Fig. 2 illustrates communication of multimedia data on Ethernet LAN environment between end systems.

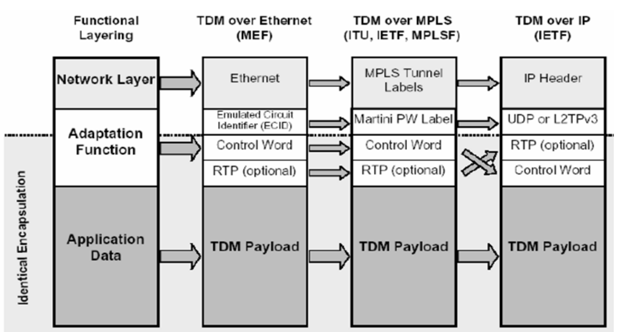

Fig. 1. Comparison of Standards [1]

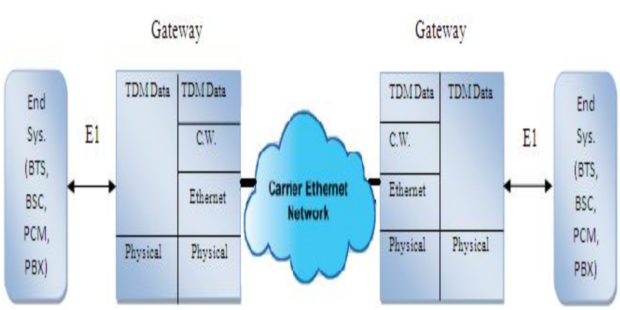

Fig. 2. Complete gateway block diagram

IV. TIME DIVISON MULTIPLEXING OVER ETHERNET (TDMOE)

For the proposed method, the TDMoE uses the LAN as an environment for transport of data. This means that TDMoE deals with layer 2 functions far from upper layer such as network, transport and application layer.

So carrying TDM over Ethernet (Not over other layer) protocol achieves many benefits:

A. Decreasing the processing delay by removing the process time of RTP, UDP and IP header.
B. Enhancing the packet efficiency by decreasing the size of header by an amount of 40 bytes for (RTP, UDP and IP) headers after remove these headers from Ethernet frame structure.
C. Decreasing the complexity and cost of the Gateway device by decreasing the frame complexity.

V. FRAME SIZE EFFECTING

The effect of frame size variation is difficult to describe theoretically because many of the parameters affecting interactive data quality (delay, loss, and jitter) are not independent and improving one parameter may cause a decline in another. Some effects of frame size on speech quality are very clear, others are less evident. Four main relationships are identified:

- A loss of a single “long” frame has more important negative effect on TDM information quality than a random loss of several “short” frames.
- Increasing frame size leads to reduce of the IP rate per call. This possibly will reduce congestion in the network and get better the quality of communication.
- In presence of data traffic in the network, increase of TDM frame size decreases link utilization, but increases the data-to-TDM traffic ratio. This can cause additional “instability” in the network, which may result in higher jitter, loss or delay. This factor may affect the resulting TDM information quality, but it might be not clear how significant the effect. It is seen that increasing frame size leads to different effects on the TDM information quality.
- Increasing frame size leads to an increase of end-to-end delay. If the delay is important, an additional increase of frame duration may be noticeable. But, if the delay is not too large, the direct impact of frame size increase is very small and not perceptually noticeable [12, 13].

VI. THE PROPOSED GATEWAY ARCHITECTURES

The main architectures of the proposed Gateway consist of five units as shown in Fig. 3. It operates in two modes these are General TDM data mode and Active TDM data mode. General mode holds to carry all time slots directly in the payload field. Active mode holds to carry the active time slots only in the payload field.

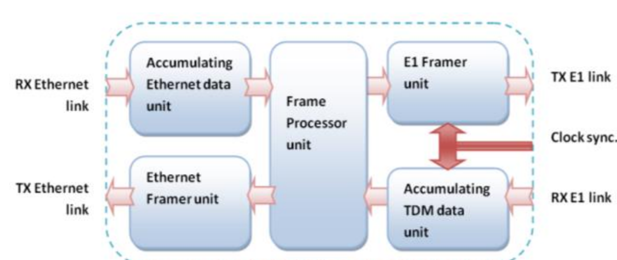

Fig. 3. General block diagram of proposed Gateway

The units of the proposed Gateway are:

A. The frame Processor unit, which carries out two operations. The first operation is receiving the TDM data from accumulating TDM unit, adding sequence header and inserting them in Ethernet payload field. To this payload field Ethernet headers are added. These headers are destination address, source address, and type/length field. CRC is also added to the frame after being calculated as a trailer. This frame containing physical headers (SFD and preamble) field is transferred to the Ethernet framer unit.
   In the second operation the Ethernet frame is received from the accumulating Ethernet unit. Matching the destination address and source address, the CRC will be checked and if valid the next process of de-capsulation and recovery of TDM data is starting. After that, the TDM data will be sent to the E1 framer unit.

B. Accumulating TDM unit receives data from RX E1 link to convert the data from serial to parallel. This unit represents the S/P converter unit and then the data sent to the unit frame Processor unit.

C. Accumulating Ethernet Unit receives the frame serially from the RX Ethernet link to convert it from serial to parallel. This unit represents the S/P converter which sends the Ethernet frame to the unit frame Processor unit.

D. E1 framer Unit receives the E1 frames from a frame processer Unit loading them serially in synchronous with the Clock sync. to the TX E1 link.

E. Ethernet framer Unit receives Ethernet frames from frame processer Unit to be loaded serially on the TX Ethernet link when the link is idle.

Processing to be applied on serial data bits from RX E1 link to TX Ethernet link is explained as flow chart shown in Fig. 5. CRC value is calculated partially after reaching each E1 frame at the frame processor unit, coming from accumulating TDM data unit. DA, SA, Length, and sequence headers are encountered in the partial calculation of CRC value before the first E1 frame only. On receiving of the remaining seven E1 frames the calculation of the CRC value will be completed. This value will be inserted in the CRC field. Partial calculation of CRC value results in reduction of processing time.
These processes included in General mode.
In active mode the E1 frame is compressed to be composed of (active frame + control word). At the partial calculation of CRC value the control word value will be checked if is equal to zero, the (active frame + control word) is replaced by one bit (X = 0) and if not the bit (X = 1) will be added to (active frame + control word) in the partial calculation of CRC value. On receiving of the remaining seven E1 frames the calculation of the CRC value will be completed. This value will be inserted in the CRC field.
After adding physical headers, Ethernet frame is completed. The final stage of GW TX is the P/S conversion of the Ethernet frame and loading on the TX Ethernet link when link was idle. It can be noted that the sequence value will increment to be compared with maximum value as shown the flow chart of Fig. 5. The Ethernet frame format explained in Fig. 4 represents the output of GW TX processes.

Preamble header	SFD header	Destination address	Source address	T/L header	Payload	CRC header
7 byte	1byte	6 byte	6 byte	2 byte	variable	4 byte

Fig. 4. Ethernet frame fields

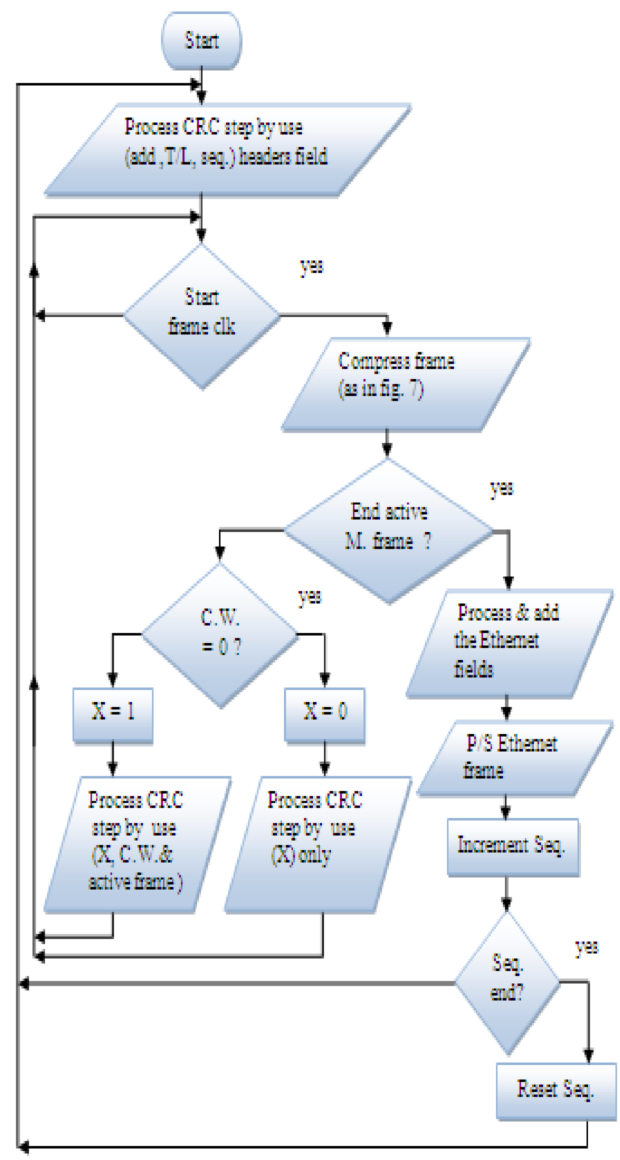

Fig. 5. G.W. TX at Active M. frame mode

In the same manner, processing to be applied on serial data bits from RX Ethernet link to TX E1 link as shown in Fig. 6. The Ethernet frame bits is converted from serial to parallel by the accumulating unit directly after removing the physical headers. The CRC value is calculated after matching each destination address and source address. If the addresses are valid, the CRC value will be checked if is equal to zero the payload is used to recover the E1frames and if not, or addresses not match, the Ethernet frame (payload) will be neglected. In general mode the E1 frames are recovered from payload directly without any process. In active mode the E1 frames are recovered from (active frames + control words) by de-compression process. De-compression process will be explained in detail later. By this, E1 frames are recovered. The final stage of GW RX is the P/S conversion of the E1 frames and loading on the TX E1 link serially in synchronous with clock sync.

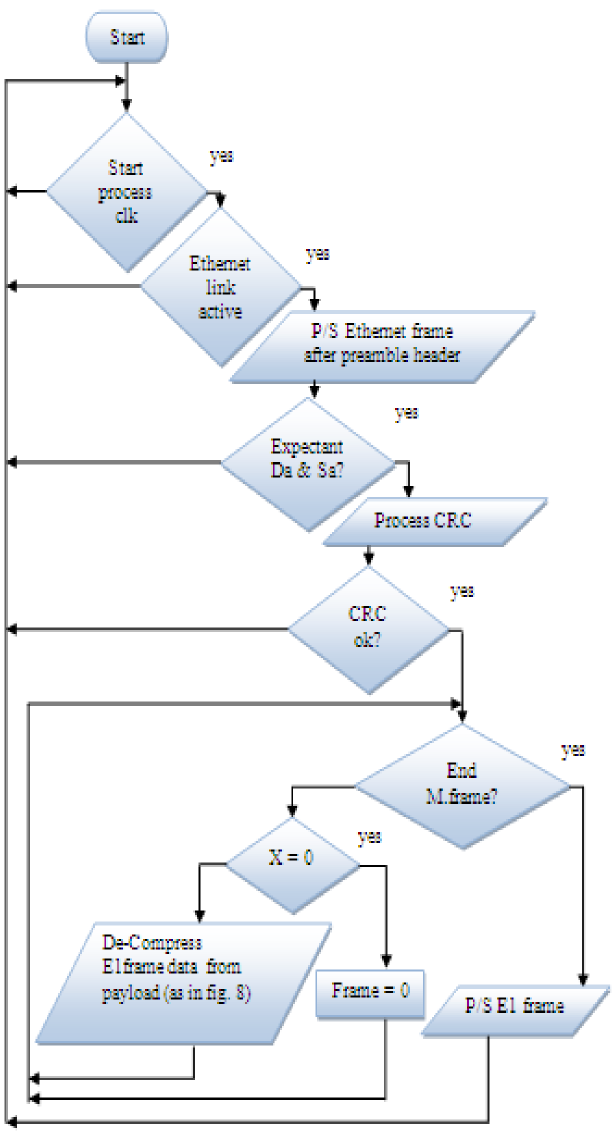

Fig. 6. G.W. RX at Active M. frame mode

VII. Comperssion and De-Comperssion Operation

The active TDM data mode includes a compression process for the E1 frame. The compression stage use statistical time-division multiplexing type in which active time slots are dynamically allocated into active frame field to improve Ethernet frame efficiency. In active frame, the number of time slots in each active frame is less than E1 frame, so the active frame length will be shorter. But, to recover data, the active frame needs the address of the location of all time slots. The control word (C.W) will represent this address. Each time slot need one bit to determine the activation and position, so the length of control word is 32 bit for 32 time slot of E1 frame. In compression stage, there is no fixed relationship between the inputs and outputs length of frame because there are no pre assigned or reserved slots. For example, if E1 frame at the input is

(09875638002100070054910000001799000080000005400000084001200001800) hex

then the C.W. and active frame respectively will be: (75632352), (875638210754911799800540548412 18)

This example shows a major difference between E1frame and active frame and C.W. This compression process is allows the recovery of the original E1 at de-packetization stage, which can be applied to all types of information from TDM data. Compression process is explained in Fig. 7. By the same manner the original E1 frame will recovered depending on address field (C.W.) at de-packetization stage as explained in Fig. 8.

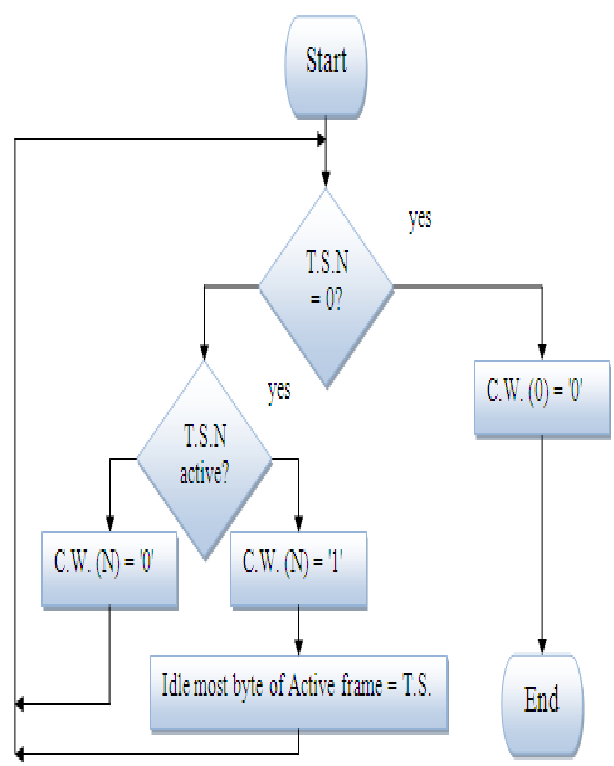

Fig. 7. Compression process

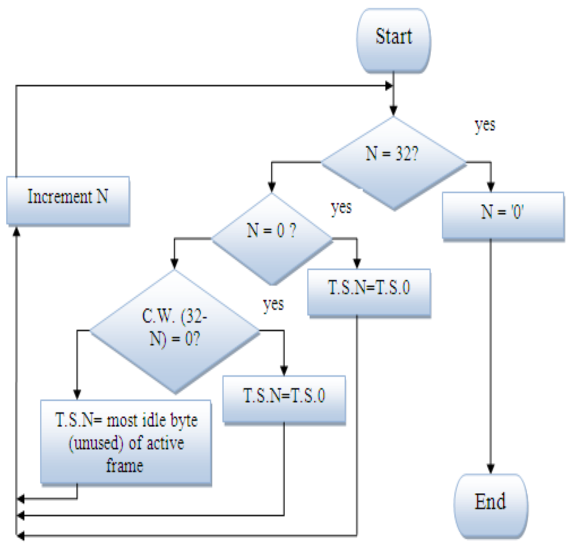

Fig. 8. De- compression process

VIII. Model Analysis

This section introduces an analysis for the proposed gateway model in terms time delay, frame error, and protocol performance.

A. System Test Bench

One of the proposed test system parts is Real time slot simulator for E1 link generator explained in Fig. 9. This block generates the E1 frame with active time slot and active E1frame ratios controlled by software settings. E1 frame will generates time slots by steps (1-32). M. E1 frame (8 E1 frame) will generates E1 frames by steps (1-8).

E1 frame received by GW TX model and send it as Ethernet frame via serial link to GW RX model.

The E1 frames will be received at this stage and the performance evaluation in terms of time delay and frame error are performed.

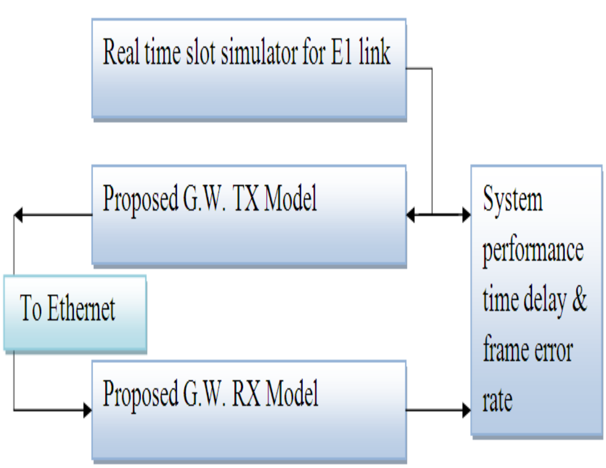

Fig. 9. The proposed test system

B. Protocol performance analysis

The factors of throughput, delay, loss, transport rate, frame efficiency, and frame size will limit the performance level. The proposed technique uses eight E1 frame in payload. In general mode, it gives (1 ms) transport rate, (2.2 Mbps) throughput, (90%) frame efficiency, and (275) frame size. The frame size takes 20% only from total length of Ethernet frame but the benefit was reducing the loss effect by ratio 20:1 comparing with G.711 code. In active mode, it gives same results with improvement in throughput with value depending on active ratio of time slots and E1frames together. Active time slots ratio and active E1 frames ratio limits the frame size and frame efficiency.

IX. Experimental Results

Large difference length of Ethernet frame is appeared in the Figs. 10 and 11 at 0% and 100% active ratio. The process delay is clearly longer at 100% active ratio comparing with 0% active ration situation.

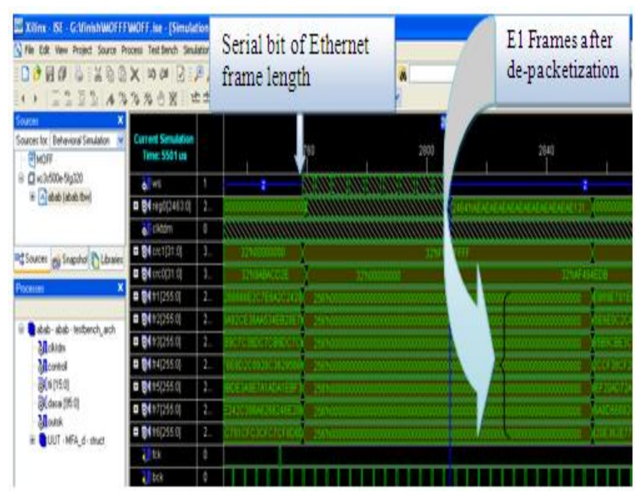

Fig. 10.. Ethernet frame signal at (100%) active ratio

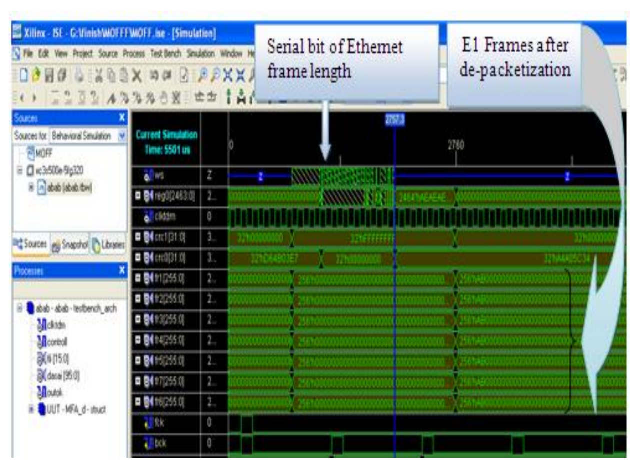

Fig. 11. Ethernet frame signal at (0%) active ratio

Fig. 12 shows the relation between the bandwidth and the no. of active byte (time slot) for general mode and active mode for different ratios. From the figure, it can be deduced that there is bandwidth saving for active mode. It can be seen that there is benefit of bandwidth saves for all frame active ratios compared with general mode. Only for the case in which the no. of active byte is more than 25 and frame active ratio 100%, the required bandwidth for active mode is greater than required bandwidth of general mode.

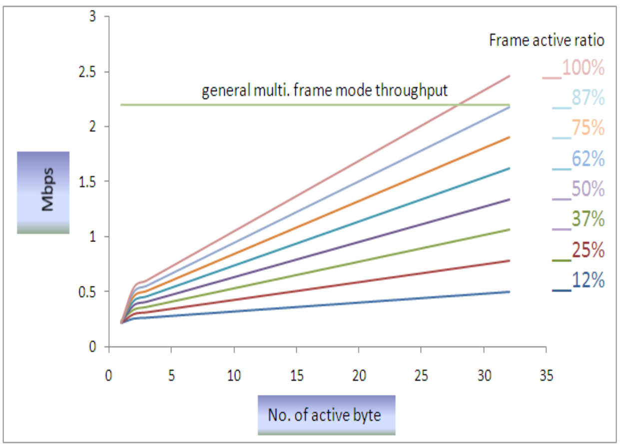

Fig. 12. Throughputs vs. Active ratio

X. Conclusions

In this paper, the applications of E1 over Ethernet protocol convertor are introduced and the features of Ethernet frame are analyzed. A new E1 over Ethernet protocol is presented as a gateway matching different network technologies. The proposed gateway is implemented using VHDL.

The time delay and the bandwidth reduction of the designed protocol convertor was tested and analyzed under different load ratios of E1 link. It is shown from the results that the required bandwidth is improved when Ethernet frames ware compressed specially when the E1 frame not fully loaded (active frame ratio below 87%) . Because the accumulating delay, the proposed Gateway has some limitation on the maximum Ethernet payload size such that the process delay not exceed 200 ms.

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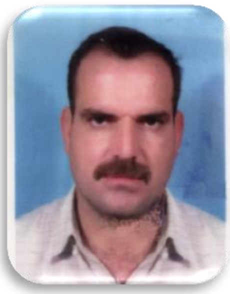

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d. Network Security 1 and Network Security 2

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